MODELS VC-6025/6045 DIGITAL STORAGE

HITACHI

SERVICE MANUAL

Hitachi Denshi, Ltd.

MODELS VC-6025/6045

DIGITAL STORAGE OSCILLOSCOPES

SERVICE MANUAL

Hitachi Denshi, Ltd.

WARNING

The service manual is prepared for qualified service personnel only. Do not perform any servicing if you are not qualified service personnel to avoid possible personnel injury, electrical shock, exposure to X-radiation, fire and other hazard.

Take X-radiation protective measures for personnel during servicing to reduce the risk of possible exposure to X-radiation.

Replace with a CRT and other critical components of the same type number and the same rating for continued safety.

SERVICING PRECAUTIONS

Read all instructions in the service manual and safety markings on the product thoroughly before servicing.

Disconnect power cord from power source before opening the enclosure.

- NOTICE -----

This Service Manual describes the most typical product of this model. If there are any specific differences between this Manual and the servicing unit, please contact Hitachi Denshi sales office in your area.

"WARNING - THESE SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT PERFORM ANY SERVICING OTHER THAN CONTAINED IN THE OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO."

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1. SPECIFICATIONS

The following specifications are applicable to the VC-6025, and VC-6045 oscilloscopes unless otherwise noted.

O CRT

Graticule: 6-inch, with internal graticule 0%, 10%, 90% and 100% markers $8 \times 10 \text{ DIV}$ (1 DIV = 1cm) Phosphor: P31 Accelerating potential:17 kV approx. (12 kV approx. for the VC-6025) External intensity modulation: Coupling: DC coupling Voltage: 5 V or more Maximum input voltage: 30 V (DC+AC peak) or 30 Vp-p AC at 1 kHz or less Bandwidth: DC to 5 MHz

O VERTICAL DEFLECTION SYSTEM

Sensitivity:	2 mV/DIV to 5 V/DIV ±3%
	(switchable in 11 steps)
	Continuously variable
Bandwidth:	DC to 100 MHz -3dB
	(DC to 50 Hz -3dB for the VC-6025)
	2 mV/DIV : DC to 20 MHz -3dB
	(DC to 10 MHz -3 dB for the VC-6025)
	AC low pass : 10 Hz -3 dB
Rise time:	3.5 ns approx.
	2 mV/DIV : 17.5 ns approx.
	(35 ns approx. for the VC-6025)
Delay time:	Leading edge can be monitored

Maximum input 400 V (DC+AC peak) at 1 kHz or less voltage: Input coupling: AC, DC, GND 1 MΩ ±1.5%, 23 pF ±3 pF Input impedance: CH1, CH2, DUAL, CHOP Display modes: (250 kHz approx.), ADD (DIFF mode can be established when the CH2 is in the INVERT mode.) Bandwidth limiting 20 MHz (10 kHz for the VC-6025) function: +, - (CH2 only) Polarity selection Common-mode rejection 20 dB minimum at 20 MHz ratio: REAL TIME mode: X-axis, X-Y operation: Y-axis selectable X-axis = CH1STORAGE mode: Y-axis = CH2X axis: CH1, CH2 2 mV to 5 V/DIV ±5% Sensitivity: 0.1 V/DIV ±5% EXT EXT:10 1 V/DIV ±5% Y axis: 2 mV to 5 V/DIV ±3% 3° or less from DC to 50 kHz Phase error: DC to 500 kHz (-3 dB) X bandwidth:

O HORIZONTAL DEFLECTION SYSTEM

Sweep time
* REAL TIME mode
A(main) sweep: 50 ns/DIV to 0.5 s/DIV
Continuously variable (UNCAL)
B(delay) sweep 50 ns/DIV to 50 ms/DIV
* STORAGE mode
A(main) sweep: 50 ns/DIV to 50 s/DIV
50 ns/DIV to 2 µs/DIV available

	only for a repetitive waveform
	0.2 s/DIV to 50 s/DIV only for
	ROLL mode
B(delay) sweep:	2.5 µs/DIV to 50 ms/DIV
	(5 $\mu s/\text{DIV}$ to 50 ms/DIV for the VC-6025)
Accuracy:	X1: ±3%, X10 MAG: ±4%
Holdoff time:	Variable
Delay time:	1 μs to 5s
Delay jitter:	1/20,000 or less
Sweep magnification:	X10
Maximum sweep rate:	5 ns/DIV
Alternate separation:	Variable (REAL TIME only)
Trigger lock function:	Provided
Auto range function:	Provided

o TRIGGERING

Trigger mode:	Trigger, auto	o trigger	
Trigger source:	CH1, CH2, EXT	T (AC,DC,DC:10), LINE	
TV trigger:	Exclusive sync separator circuit		
	provided		
	Sensitivity:	SYNC signal	
	INT:	1 DIV or more	
	EXT:	200 mVp-p or more	

Trigger sensitivity:

NORM mode:

Frequency	DC to 20 MHz	20 to 100 MHz (20 to 50 MHz for the VC-6025)	
INT	0.35 DIV	1.5 DIV	
EXT	50 mV	150 mV	

AUTO mode:

Slope:

Frequency	30 to 100 Hz	100 Hz to 20 MHz	20 to 100 MHz (20 to 50 MHz for the VC-6025)
INT	1.5 DIV	1 DIV	1.5 DIV
EXT	150 mV	100 mV	150 mV

Trigger level variable range: AUTO: Automatically corresponds to

the trigger signal
NORM:
INT: ±4 DIV or more
EXT: ±0.4 V or more
EXT:10:±4 V or more
+, -
Impedance: 1 M Ω ±5%, 25pF ±6 pF
Voltage: 400 V (DC+AC peak) at 1 kHz

O READOUT FUNCTION

External input:

Panel setting display:	Vertical axis: V/DIV, UNCAL, probe conversion
	Sweep speed: S/DIV, UNCAL, MAG (converted value)
	Other: Delay time, X-Y, TRIGGER, No. of averaging

O CURSOR READOUT

Function:	Voltage difference ΔV : Δ -REF
	Time difference ΔT : $\Delta-REF$
	Frequency $1/\Delta T$: Δ -REF

O EXTERNAL OUTPUT

Trigger signal out: Output voltage : 25 mV/DIV approx. (Full scale on the CRT) 50-ohm termintation Frequency response: DC to 10 MHz (-3 dB) Output impedance : 50 ohms approx.

O CALIBRATOR

Waveform:	1 kHz	±20%,	square	wave
Voltage:	0.5 V	±1왕		

DIGITAL STORAGE FUNCTIONS

O WAVEFORM DATA STORAGE

```
Memory capacity
       Display memory: 1000 words x 4
       Save memory:
                       1000 words x 2
       Acquisition
       memory:
                        Single trace 2.5 µs/DIV to 50 s/DIV
                                      --- 4000 words
                                      (5 µs/DIV to 50 s/DIV
                                      --- 2000 words for
                                          the VC-6025)
                                      50 ns/DIV to 2 µs/DIV
                                      --- 1000 words
                       Dual trace
                                      2.5 µs/DIV to 50 s/DIV
                                      --- 2000 words/CH
                                      5 \mus/DIV to 50 s/DIV
                                      --- 2000 words/CH for
                                          the VC-6025
```

50 ns/DIV to 2 us/DIV --- 1000 words/CH Vertical resolution: 8 bits/10 DIV Horizontal resolution: 100 data/DIV Maximum sampling rate: 40 Msps, one-channel sampling VC-6045: 40 Msps, two-channel alternate sampling 20 Msps, two-channel alternate VC-6025: sampling Sampling rate depends on the time range. Maximum storage frequency: A single-shot signal (Maximum amplitude error 5 MHz 30% or less): A repetitive signal: 100 MHz (20 MHz at 2 mV/DIV) VC-6045: 50 MHz (10 MHz at 2 mV/DIV) VC-6025: O DATA ACOUISITION storage mode: Updates a picture on the CRT at each NORM triggering. Averages input signals by the selected AVG mode: number of sweeps and displays the result after the averaging has reached the selected number. (Number of average: 4 or 16) Shifts data from right to left contin-ROLL mode: uously on the CRT. (The updating point is the right end.) Holds the waveform displayed on the CRT. HOLD mode: an operation of the NORM Performs SINGLE sweep: each at or AVG mode once storage. pressing the SINGLE RESET switch in the HOLD mode, and updates a picture.

o DATA SAVE: Up to two waveforms can be saved. Two stored waveforms forms can be displayed with the two sampling waveforms.

o PRETRIGGER: Variable (in 0.1 DIV steps)

- o PLOTTER OUTPUT: Hard copy is available by the HP-GL through RS-232C. 6 colors are switchable.
- o EXT INPUT: Provided with the RS-232C interface as standard.
- o MAGNIFYING DISPLAY: A storage waveform can be magnified up to 10 times in the horizontal direction.
- o MEMORY BACK-UP: Only a save memory can be backed up for approx. 48 hours.

O POWER SUPPLY

Voltage:	90 V to 250 V AC
Frequency:	48 to 440 Hz
Power consumption:	50 W approx.

O ENVIRONMENT

Operating temperature:	0 to 40 ^o C
Operating humidity:	45 to 85%
Specification guaranteed	
temperature:	10 to 35 ⁰ C
Safe storage temperature:	-20 to +70 ⁰ C
Safe storage humidity:	35 to 85% (70% or less in the
	ambient temperature of 50 ⁰ C)

O DIMENSIONS AND WEIGHT

Dimensions:	275(W) x 130(H) x 360(D) mm
	approx.
	(10.8(W) x 5.1(H) x 14.2(D) in.
	approx.)
Weight:	7 kg approx. (15.4 lb. approx.)

2. ACCESSORIES

The VC-6025/VC-6045 Digital Storage Oscilloscopes are shipped with the following standard accessories:

- 2 Probes (AT-10AP1.5)
- 1 AC Power Cord
- 1 Operation Manual
- 1 Fuse (2A)

3. PREVENTIVE MAINTENANCE

Preventive maintenance, when performed on a regular basis, can prevent instrument breakdown and may improve the reliability of the oscilloscope. The severity of environment to which this instrument is subjected will determine the frequency of maintenance. A convenient time to perform preventive maintenance is preceding recalibration of the instrument.

Disassembly

Remove the top cover and the bottom cover of the instrument. Most of the internal parts of the instrument are now accessible. If access to the front of the circuit boards are necessary, remove the knobs from the external control shafts on the board.

Cleaning

The instrument should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause component breakdown.

The covers provide protection against dust in the interior of the instrument. Loose dust accumulated on these covers can be removed with a soft cloth or small brush.

Dirt that remains can be removed with a soft cloth dampened in a mild detergent and water solution. Abrasive cleaners should not be used. Cleaning the interior should only be occasionally necessary. The best way to clean the interior is to blow off the dust with a dray, low-velocity stream of air. A soft-bristle brush or a cotton-tipped applicator is useful for cleaning in narrow spaces or for cleaning more delicate components.

Visual Inspection

The instrument should be inspected occasionally for such defects as broken connections, improperly seated transistors, damaged circuit boards, and heat-damaged parts. The corrective procedure for most visible defects is apparent; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; therefore, correcting the cause of the overheating is important to prevent recurrence of the damage.

4. CALIBRATION

Hitachi Denshi provides complete instrument repair and calibration. Contact your local Hitachi Denshi office or representative.

4.1 Calibration interval

To maintain instrument accuracy, perform the calibration of the VC-6025/6045 at least every 1000 hours of operation or every six months if used infrequently.

4.2 Test equipment required

The test equipment and accessories listed in Table 4-1 or equivalent are required to perform the calibration of the VC-6025/6045. The minimum specifications required for accurate calibration are also listed. All the test equipis assumed to be correctly calibrated and ment operate properly within the listed specifications. It is recommended to use the test equipment which exceeds the listed specifications. Operating instructions for the test equipment are not given in this procedure. Refer to the instruction manual for the test equipment for more information.

4.3 Preliminary procedure

This instrument should be calibrated at an ambient temperature of $+20^{\circ}C$ ($\pm 5^{\circ}C$) for the best overall accuracy.

- (1) Connect the instrument to AC line voltage, 50 Hz to 400 Hz line source.
- (2) Set the instrument controls as given in the Preliminary Control Settings. Allow at least fifteen minutes of warmup before proceeding.
- (3) See the Adjustment Locations in Section 6.

Table 4-1TEST EQUIPMENT AND ACCESSORIES REQUIRED

		IESI EQUIPMENI AND ACCEDUCATE	~ ~ ~ ~	
	Description	Specifications	Applications	Examples of Applicable Test Equipment
1	Constant Amplitude Signal Generator	Reference frequency: 50 kHz, Maximum frequency: 150 MHz, Amplitude: variable	Check horizontal, vertical and trig- ger bandwidths.	TEKTRONIX R SG503
2	Standard amplitude Calibrator	Amplitude accuracy: 0.25%, Variable amplitude: 5 mV to 40 V, Frequency: 1 kHz square wave	Check horizontal and vertical gains.	TEKTRONIX PG506
3	Square-wave Generator	Variable frequency: 10 Hz to 1 MHz, Output amplitude: 10 mV to 100 V	Check probe and vertical compensa- tion.	TEKTRONIX PG506
4	Digital Multimeter	Accuracy: 0.1%	Check power supply.	TEKTRONIX DM501A
5	Digital Frequency Counter	Accuracy: 0.1%	Check CAL frequency.	
6	Time Mark Generator	Accuracy: 0.1%	Check sweep time.	TEKTRONIX TG501
7	Cable	Impedance: 50 ohms, Type: RG-58/U, Length: 42 inches, Connectors: BNC	This cable is used for almost all adjustment.	Hitachi Part No. 4202
8	Termination	Impedance: 50 ohms, Connectors: BNC Feed through	Check vertical amplifier compensation.	
9	Attenuator	Ratio: 10X, Connectors: BNC, Impedance: 50 ohms	Check vertical amplifier bandwidth.	
10	T-Connector	Connectors: BNC	Check X-Y operation.	Hitachi Part No.1301

4.4 Preliminary control settings

Set the instrument controls as follows, when starting the calibration procedures.

Controls		Setting
POWER		OFF
FOCUS		Midrange
TRACE ROTATI	ON	Any position
INTEN		CCW
READOUT INTE	N	CCW
V. POSITION	CH1 CH2	Midrange Midrange
V. VAR	CH1 CH2	CW (CAL) CW (CAL)

Controls		Setting	
AC-DC	CH1 CH2		position position
GND	CH1 CH2	GND GND	
SELECTO	R	Any	position
VARIABL	ES	Any	position
TIME/DIV		Any	position
H MODE		А	
V MODE		CH1	

Note:

CW: Clockwise CCW: Counterclockwise V MODE: Vertical mode

H MODE: Horizontal mode

After completion of the above settings, turn the POWER control to ON, and set the INTEN and READOUT INTEN controls to any position.

4.5 Initial starting procedure

- (1) Turn instrument POWER on.
- (2) Allow a few seconds for the cathode ray tube (CRT) to warm up. A trace will appear on the display of the CRT.
- (3) If trace does not appear, increase the intensity by the INTEN control clockwise rotation until the trace is easily observed.
- (4) Adjust FOCUS control for optimum focus.
- (5) Adjust POSITION controls to center the trace if necessary.

POWER SUPPLY

+12 V ADJ RV1506 (PEF-784) Measure the voltage on pin 3 of connector P1501 on the PEF-784 board with a digital voltmeter, and adjust RV1506 so that the voltage is +11.975 to +12.025 V. RV1042 (PEF-784) CRT BIAS Set: a. CH1 MODE: SOURCE OR X : CH2 GND (CH1, CH2): ON (Push-in) X-Y (Simultaneously push ALT and B.) H MODE: SELECTOR: H POS EXT INPUT (for X signal): No signal

- b. Position a spot at the center on the CRT screen by the CH1 POSITION (vertical position and the VARIABLES controls.)
- Note: When the SELECTOR selects H POS, the VARIABLES control is used as a horizontal position control.
 - c. Adjust the INTEN control so that the voltage on Z OUT CHECK on the PEF-784 board is +15 V.
 - d. Adjust CRT BIAS control RV1042 just before the spot starts to appear on the screen.
 - e. Adjust the INTEN control and verify that the spot starts to appear within the range (as illustrated below.)

INTEN



TRACE ROTATION RV1606 (Front Panel)

a. Set:

T.	IME/DIV:	Α:	1	ms
Η	MODE:	А		
v	MODE:	CH1		

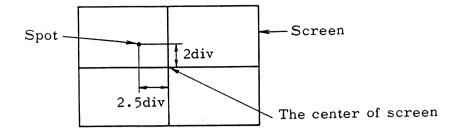
- b. Adjust the horizontal position until the left end of the trace is lined up with the center of the leftmost vertical graticule line on the screen.
- c. Adjust the TRACE ROTATION control on the front panel so that the trace is parallel with the horizontal graticule line.
- d. Repeat b and c alternately until the trace is aligned with the center horizontal graticule line.
-) ASTIG RV1281 (PEF-784)

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FOCUS RV1607 (Front Panel)
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a. Set:

CH1 GND: ON (Push-in) CH2 GND: ON (Push-in) H MODE: X-Y (Simultaneously push ALT and B.) SOURCE OR X: CH1 BW LIMIT: ON

- b. Locate a spot as illustrated in the following figure.
- c. Adjust INTEN control RV1601 (Front Panel) just before halation starts to occur.
- d. Rotate FOCUS control RV1607 (Front Panel) fully clockwise.
- e. Adjust ASTIG control RV1281 (PEF-783) so that the spot is a circule as true as possible.
- f. Adjust FOCUS control RV1607 (Front Panel) to obtain the smallest spot.



-) FOCUS CENT RV1253 (PEF-784)
 - a. Perform adjustment (4)
 - b. Set the FOCUS control to the mechanical mid-position.
 - c. Adjust FOCUS CENT control RV1253 (PEF-784) to obtain the samllest spot.

HORIZONTAL

Press AUTO of the TIME/DIV switch while holding the SELECTOR downward (∇) so that the sweep circuit operation is initialized. Then, proceed the following adjustment. (The adjustment in the X-Y mode is simultaneously performed.)

6) H GAIN RV834 (PEF-782)

a. Set:

5

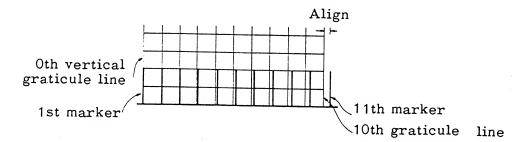
CH2 AC/DC:	AC
CH2 VOLTS/DIV:	10 mV (CAL)
H MODE:	X – Y
V MODE:	CH1
SOURCE OR X:	CH2
CH1 GND:	GND (Push-in)

b. Connect a 50 mV square wave to the CH2 INPUT connector.

c. Adjust H GAIN control RV834 (PEF-782) so that the distance between the spots on the CRT is 5 div.

7) 1 ms/div ADJ RV801 (PEF-782) a. Set: V MODE: CH1 CH1 AC/DC: DC H MODE: А A TIME/DIV: A = 1 msCH1 input: 1 ms time mark signal from a time mark generator INTEN: As required READOUT INTEN: As required x10 MAG: OFF

- b. Align the 1st time marker with the zeroth (leftmost) vertical graticule line.
- Note: This adjustment is performed by moving the horizontal position by the VARIABLES control with H POS selected by the SELECTOR.
- c. Adjust 1 ms/div ADJ control RV801 (PEF-782) so that the 11th time marker is aligned with the 10th (rightmost) vertical graticule line.



x10 MAG GAIN RV844 (PEF-782)

a. Set:

V MODE: CH1 CH1 AC/DC: DC H MODE: А CH1 input: 1 ms from the time mark generator INTEN: As required REDOUT INTEN: As required x10 MAG: ON A * 0.1 ms (since the x10 MAG control A TIME/DIV: is ON)

- b. Align the 1st time marker with the zeroth (leftmost) vertical graticule line.
- c. Adjust MAG GAIN control RV844 (PEF-782) so that the 11th time marker is aligned with the 10th (rightmost) vertical graticule line.
- 9) MAG CENT RV831 (PEF-782)
 - a. Set:

Same as adjustment (8) - a.

- b. Adjust the horizontal position, and align the rising portion of the 2nd time marker with the center vertical graticule line (6th line from the left).
- c. Adjust MAG CENT control RV831 (PEF-782) so that the above 2nd time marker is not displaced from the center vertical graticule line when the X10 MAG switch is set to off.

(10) H POS START RV807 (PEF-782)

- a. Set the POWER switch to OFF first, and then turn it back to ON. At this time, leave the controls on the front panel as they are.
- b. Adjust H POS START RV807 (PEF-782) so that the start point of the sweep is aligned with the leftmost graticule line.

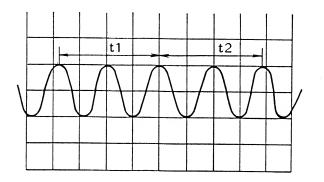
(11) 5 ns CV859 (PEF-784)

a. Set: A TIME/DIV: A = 50 ns

- CH1 input: 10 ns (Fed from the time mark generator) (When the rate is 10 ns or more, a sinewave is supplied.)
 - H POS: Adjust so that the numbers of the peaks on either side of the center vertical graticule line are equal

x10 MAG: ON

- b. Adjust the H POS control so that the numbers of the peaks on either side of the center vertical graticule line are equal with the peak of the center wave aligned with the center vertical graticule line.
- c. Adjust 5 ns CV859 (PEF-784) so that the time $(t_1 \text{ and } t_2)$ from the center vertical graticule line to the 2nd peaks on either side of the center line is equal.



VERTICAL

2) CH1 DC BAL RV37 (PEF-781)

a. Set:

V MODE: CH1 CH1 GND: ON (Push-in) CH1 VOLTS/DIV: 2 mV A TIME/DIV: A = 1 ms CH1 V POSITION: Mid-position

b. Adjust CH1 DC BAL control RV37 (PEF-781) so that the displacement of the trace is within ±0.1 div when the CH1 VOLTS/DIV switch is switched between 2 mV and 10 mV.

B) CH2 DC BAL RV137 (PEF-781)

a. Set:

V MC	DDE:	CH2	2
CH2	GND:	ON	(Push-in)

CH2 VOLTS/DIV: 2 mV A TIME/DIV: A = 1 ms CH2 V POSITION: Mid-position

- b. Adjust CH2 DC BAL control RV137 (PEF-781) so that the displacement of the trace is within ±0.1 div when the CH2 VOLTS/DIV switch is switched between 2 mV and 10 mV.
- (14) CH2 POS CENT RV162 (PEF-781)
 - a. Set:

V MODE: DUAL V POSITION: Mid-position (CH1, CH2) GND (CH1, CH2): ON (Push-in) A TIME/DIV: A = 0.1 ms

- b. Adjust CH2 POS CENT control RV162 (PEF-781) so that the trace does not move when CH2 INV control S1611 (PEF-783) is turned on and off.
- 15) CH1 POS CENT RV62 (PEF-781)
 - a. Set:

V MODE: DUAL

CH2 V POSITION: As set in (14) - a. CH2 GND: ON (Push-in)

b. Adjust CH1 POS CENT control RV62 (PEF-781) so that the trace is aligned with the CH2 trace (See item (13)).

16) CHR Y CENT RV574 (PEF-785)

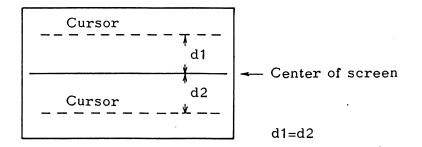
a. Set:

Turn the POWER switch to OFF first, and then back to ON to initialize the microcomputer. CHR INTEN: As appropriate V MODE: CH1 CH1 VOLTS/DIV: 10 mV (H MODE: A)

SELECTOR: ΔV of MEASURE

When power is turned on, H POS is automatically set. Consequently, when the SELECTOR switch is lowered one step further, MEASURE is selected (the LED lights) and Δ^{V} is displayed on the screen. (If the SELECTOR switch is lowered one more step, Δ^{T} is displayed on the screen with the MEASURE LED lit. If the switch is lowered one more step, $1/\Delta^{T}$ is displayed on the screen.) VARIABLES: Do not touch to avoid a possible movement of the cursors.

- b. Verify that the " $\Delta V{=}60.00~mV$ " is displayed at the top left of the screen.
- c. Adjust CHR Y CENT RV574 (PEF-785) so that the cursors are at the same distance from the center of the screen.

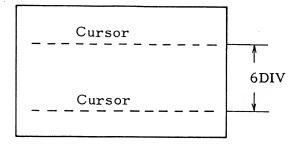


) CHR Y GAIN RV576 (PEF-785)

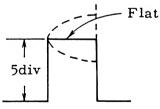
a. Set:

Same as (16) (1).

b. Adjust CHR Y GAIN RV576 (PEF-785) so that the distance between the two cursors is 6 div.



CHR Y CENT RV574 (PEF-785) the CHR Y GAIN adjustment is related to the CHR Y Since CENT adjustment, adjust the CHR Y CENT adjustment described (16)again. in CH1 DC GAIN RV30 (PEF-781) a. Set: VERT MODE: CH1 CH1 VOLTS/DIV: 10m V/DIV TIME/DIV: A = 1 msCH1 AC-DC: DC CH1 input: 1 kHz, 50 mVp-p square wave (from the Tektronix's pulse generator PG-506 or equivalent) Set the PG-506 in the FAST RISE mode and connect the output (1 kHz square wave) in the 50-ohm termination. (In the FAST RISE mode, a waveform with a flat top is ensured.) Adjust the pulse generator so that the amplitude of the b. square wave is appprox. 5 div at the center on the screen. (50-ohm terminated) Adjust CH1 DC GAIN control RV30 (PEF-781) so that the с. square wave is flat at top.



) CH2 DC GAIN RV130 (PEF-781)

a. Set:

20

VERT MODE: CH2 CH2 VOLTS/DIV: 10mV/DIV

A TIME/DIV: A = 2 msCH2 AC/DC: DC CH2 input: Same as CH1 input (19) or equivalent Adjust the pulse generator so that the amplitude of the b. square wave is approx. 5 div on the screen. Adjust CH2 DC GAIN control RV130 (PEF-781) so that the с. square wave is flat at top. V GAIN RV505 (PEF-785).... Total gain control common to CH1 and CH2 Set: a. MODE: CH1 SOURCE OR X: CH2 TRIG MODE: AUTO (Free-running scan) Normally free-running scan is performed in the AUTO mode unless the trigger level is at the fringe of triggering. If the free-running scan is not performed, adjust the TRIG LEVEL control. CH1 VOLTS/DIV: 10 mV A TIME/DIV: A = 0.1 msCH1 input: 1 kHz, 50 mVp-p square wave for calibration (from PG-506 on equivalent) (50-ohm termination open) b. Adjust V GAIN control RV502 (PEF-785) so that the amplitude of the square wave is 5 div at the center on the screen.

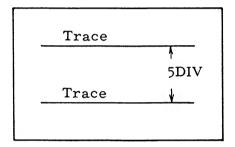
Trace	
	Ť
	5DIV
Trace	¥
	·····

22) CH2 GAIN control RV133 (PEF-781)

a. Set:

MODE:	CH2
SOURCE OR X:	CH1
TRIG MODE:	AUTO (Free-running trace)
CH2 VOLTS/DIV:	10 mV
A TIME/DIV:	A = 0.1ms
CH2 input:	Same as CH1 input (21)

b. Adjust CH2 GAIN control RV133 (PEF-781) so that the amplitude of the square wave is 5 div at the center on the screen.

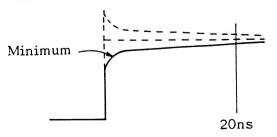


23) CH1 HF COMP CV517, CV556, CV515 (PEF-785)

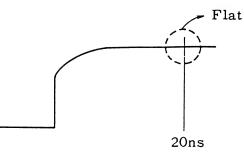
a. Set:

V MODE:	CH1
CH1 AC/DC:	DC
CH1 VOLTS/DIV:	10 mV/DIV
CH1 input:	Tektronix's pulse generator PG506 or
	equivalent when the PG506 is in the
	FAST RISE mode, a square wave (Tr ≤ 1
	ns) is obtained. Connect this signal
	to CH1 in 50-ohm termination.

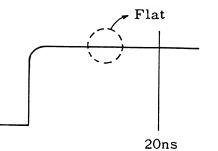
b. Adjust CV517 so that the amplitude around the rising edge is minimum.



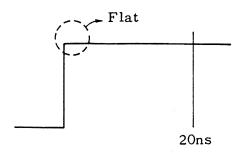
c. Adjust CV515 so that the portion near 20 ns is flat.



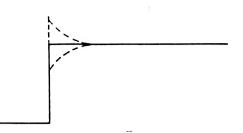
d. Adjust CV556 so that the midway point between the rising edge and 20 ns is flat.



e. Adjust CV517 so that the portion near the rising edge is flat.



CH2 HF COMP CV160 (PEF-781) a. Set: V MODE: CH2 CH2 AC/DC SW: DC CH2 VOLTS/DIV: 10 mV CH2 input: Same as CH1 input (23) b. Adjust CV160 (PEF-781) so that the rising portion is flat.



25) CH1 ATT CV4, CV5, CV14, CV15 (PEF-781)

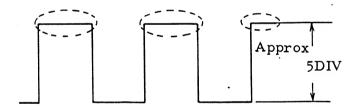
(1) Attenuation characteristics

Connect the output of the PG-506 directly to CH1.

a. Set:

V MODE:	CH1
CH1 input:	Place the PG-506in the HIGH AMPLITUDE
	range and connect the output (10 kHz
	square wave) to CH1.

- b. Set CH1 VOLTS/DIV to 0.1 V. (CH1 ATTN is set to +10.)
- c. Adjust the output amplitude control of the PG-506 so that the amplitude of the waveform is approx. 5 DIV.
- d. Adjust CV5 (PEF-781) so that the top of the waveform is as flat as possible.



- e. Set CH1 VOLTS/DIV to 1 V. (CH1 ATTN is set to ÷100.)
- f. Adjust the output amplitude control of the PG-506 so that the amplitude of the waveform is approx. 5 DIV.
- g. Adjust CV15 (PEF-781) so that the top of the waveform is as flat as possible.
- (2) Input capacitance Connect the output of the PG-506 to CH1 by a 10:1 probe.
- a. Set:

V MODE: CH1

CH1 input: Place the PG-506 in the HIGH AMPLITUDE range and connect the output (10 kHz square wave) to CH1 by the 10:1 probe.

- b. Same as b of (1).
- c. Same as c of (1).
- d. Adjust CV4 (PEF-781) so that the top of the waveform is as flat as possible.
- e. Same as e of (1).
- f. Adjust the output amplitude adjustment of the PG-506 so that the amplitude of the waveform is 1 to 2 DIV on the screen.
- g. Adjust CV14 (PEF-781) so that the top of the waveform is as flat as possible.
- 6) CH2 ATT CV104, CV105, CV114, CV115 (PEF-781)
 - Same as (25) except that the V MODE input and the VOLTS/DIV settings are changed to CH2.

CV104 corresponds to CV4 of (25). CV105 corresponds to CV5 of (25). CV114 corresponds to CV14 of (25). CV115 corresponds to CV15 of (25).

27) TRIG SIG OUT DC LEVEL RV320 (PEF-781)

a. Set:

SOURCE OR X: CH1

CH1 GND: ON (Push in)

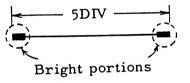
- b. Connect the digital voltmeter or the oscilloscope to TRIG SIGNAL OUT J301.
- c. Adjust RV320 (PEF-781) so that the output voltage is zero volts.

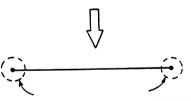
The following procedures (28 , 29 and 30) are needed for the adjustment of the frequency response of the amplifier in the TRIG system.

- 28) INT HF COMP CV305 (PEF-781)
 - a. Set:

CH1 in 50-ohm termination.

- b. Adjust the output control of the PG-506 so that the trace of approx. 5 DIV is displayed in the horizontal direction of the screen.
- c. Adjust INT HF COMP CV305 (PEF-781) so that both ends of the trace is as small as possible.





As small as possible

9) EXT 1/1 HF COMP CV306 (PEF-781)

a. Set:

		EXT DC
	-	Same as CH1 input of (28)
b.	Same as b of (28)	

- c. Adjust EXT 1/1 HF COMP CV306 (PEF-781) so that both ends of the trace are as small as possible.
- 30) EXT 1/10 HF COMP CV307 (PEF-781)
 - a. Set:

SOURCE OR X: EXT DC ÷ 10

Other settings are the same as (29) .

- b. Adjust the output control of the PG-506 so that the trace of approx. 1 DIV is displayed in the horizontal direction on the screen.
- c. Adjust EXT 1/10 HF COMP CV307 (PEF-781) so that both ends of the trace are as small as possible.

l) TRIG (+) PEAK RV685 (PEF-782)

a. Set:

SOURCE OR X:	CH1
V MODE:	CH1
TRIG MODE:	A = 20 µs
CH1 VOLTS/DIV:	10 mV or 20 mV
SLOPE:	(+)
TRIG LEVEL:	CW
CH1 input:	Square wave of approx. 50 kHz
	(4 DIV amplitude on screen)

b. The trigger point is changed as shown in dotted lines by the TRIG + PEAK control. Adjust TRIG + PEAK RV685 (PEF-782) so that the trace is triggered at as high a point as possible.

(-)

) TRIG (-) PEAK RV675 (PEF-782)

a. Set:

SLOPE:

TRIG LEVEL: CCW

Other settings are the same as (31) .

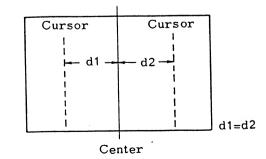
b. Adjust TRIG - PEAK RV675 (PEF-782) so that the trace is triggered at as low a point as possible.

External output

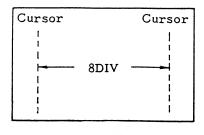
(33) PROBE ADJ RV1303 (PEF-785) Measure the PROBE COMP output at J502 by the digital voltmeter, and adjust PROBE ADJ RV1303 (PEF-785) for 0.250 V.

CHR X

- (34) CHR X CENT RV876 (PEF-782)
 - a. Set:
 - Turn the POWER switch to off first, and then back to on to initialize the microcomputer. READOUT INTEN: As appropriate SELECTOR: ΔT of MEASURE (Refer to SELECTOR of (16) a.) VARIABLES: Do not move.
 - b. Verify that "8.00 ms" is displayed on the top left of the screen.
 - c. Adjust CHR X CENT RV876 (PEF-782) so that the distances between the center of the screen and the cursors are equal.



- 35) CHR X GAIN RV884 (PEF-782)
 - a. Set: Same as (34) (1).
 - b. Adjust CHR X GAIN RV884 (PEF-782) so that the distance between cursors is 8 DIV.



NOTE:

When the power switch of this instrument is turned on, the time base calibration and the diagnosis of the sweep circuit operation are performed by the built-in microcomputer.

If the result is normal, "CALIBRATION-COMPLETED" is displayed on the CRT 20 seconds after the power has been turned on, and the instrument is placed in the standard state.

If the result is not normal, "CALIBRATION-FAILED AT SWEEP CKT (or CYCLE CKT)" is displayed. When the power switch is turned on after storage in a low temperature, allow several minutes until circuits become stable. Then turn off the power switch and turn on the switch again.

If "CALIBRATION-COMPLETED" is displayed, the operation is normal. If "CALIBRATION-FAILED AT SWEEP CKT" is displayed again, check the sweep circuit (PEF-782 or PEF-837.)

STORAGE

- (36) V CENT (STORAGE Y CENT) RV5501 (PEF-880)
 - a. Set:

STORAGE: ON (LED blinks and the storage mode is established.)

MEASURE: ΔV cursor

- b. Adjust RV5501 so that the two cursors are positioned symmetrically with respect to the horizontal center line on the CRT.
- 37) V GAIN (STORAGE Y GAIN) RV5502 (PEF-800)
 - a. Set: Same as (36)
 - b. Adjust RV5502 so that the distance between the two cursors is 6 divisions.

c. Perform the adjustment mentioned under (36) again.

- (38) H CENT (STORAGE X CENT) RV5503 (PEF-880)
 - a. Set:

STORAGE: ON (LED blinks and the storage mode is selected.)

MEASURE: AT cursor

- b. Adjust RV5503 so that the two cursors are positioned symmetrically with respect to the vertical center line on the CRT.
- (39) H GAIN (STORAGE X GAIN) RV5504 (PEF-800)
 - a. Set: Same as (38)
 - b. Adjust RV5504 so that the distance between the cursors is 8 divisions.
 - c. Perfrom the adjustment mentioned under (38) again.

(40) S/H ADJ (S/H BALANCE) RV8060 (PEF-880)

a. Set:

- STORAGE: OFF (LED goes off and the RTO mode is established.)
 Input coupling: GND (The GND switch is pushed in.)
 V MODE: CH1
 CH1 V POSITION: Align the trace with the center
 graticule on the CRT. (Fix this
 control.)
 STORAGE: ON (LED blinks and the storage mode
 is established.)
- b. Measure the voltage difference between DC LEVEL 1 and DC LEVEL 2 on the PEF-883 through the two guide holes (DC LEVEL 1 and DC LEVEL 2 are silk-screened) on the PEF-880, using the digital voltmeter.
- c. Adjust RV8060 so that the above voltage difference is less than 10 mV.

) EQS CENT (Equivalent sample start poiknt) RV5301 (PEF-880) a. Set:

STORAGE: ON (LED blinks and the storage mode is established.)

A TIME/DIV: A = 50 ns V MODE: CH1 Input coupling: GND (The GND switch is pushed in.) TRIGGER MODE: AUTO

b. Measure the voltage waveform on R5313 by the oscilloscope, and adjust RV5301 so that the sweep start voltage becomes 0.1 V.

A2) Not silk-screened (equivalent sample gain) RV5302 (PEF-880) a. Set:

Input coupling: Dc (The AC/DC switch is pused in.) Other settins are the same with $\overbrace{41}$.

- b. Connect the 50 ns marker to CH1 INPUT and trigger the signal by adjusting the TRIGGER LEVEL.(The markers stop.)
- c. Adjust RV5302 so that the distance between the first and last markers is 9 divisions.

3) AD1 GAIN (CH1 A/D GAIN) RV5201 (PEF-800)

a. Set:

SOURCE OR X: CH1 (The trigger source is CH1.) V MODE: CH1 CH1 VOLTS/DIV: 10 mV A TIME/DIV: A = 1ms Input signal: Calibration square wave (1 kHz, 50 mV) SMOOTH: OFF (Display "SMOOTH" by the MENU switch and "SMOOTH OFF" by the VARIABLES contrtol.)

- b. Establish the RTO mode, and verify that the amplitude is5 divisions in the RTO mode.
- c. Establish the STORAGE mode, and adjust RV5201 so that the amplitude is 5 divisions on the CRT.

44) AD1 NORM OFFSET (CH1 A/D OFFSET) RV5202 (PEWF-880)

a. Set:

TRIGGER MODE: AUTO

Other settings are the same with (43)

- b. Establish the RTO mode, and set the input coupling mode to GND.
- c. Position the trace at the center of the CRT by CH1 V POSITION.
- d. Establish the STORAGE mode and adjust RV5202 so that the trace is positioned at the center of the CRT.
- e. Establish the RTO mode again, and verify that the trace is positioned at the center of the CRT.

5) AD2 GAIN (CH1 A/D GAIN) RV5251 (PEF-880)

a.	Set:			
	SOURCE OR X:	CH2 (The trigger source is CH2.)		
	V MODE:	DUAL		
	CH1 input coupling:	GND (The GND switch is pushed in.)		
	CH2 VOLTS/DIV:	10 mV		
	A TIME/DIV:	A = 1 ms		
	CH2 INPUT:	Calibration square wave		
		(1 kHz, 50 mV)		
	SMOOTH:	OFF (Display "SMOOTH" by the MENU		
		switch and "SMOOTH OFF" by the		
		VARIABLES control.)		

- b. Establish the RTO mode, and verify that the amplitude is5 divisions on the CRT.
- c. Establish the STORAGE mode, and adjust RV5251 so that the amplitude is 5 divisions on the CRT.
- 46) AD2 OFFSET (CH2 A/D OFFSET) RV5252 (PEF-880)
 - a. Set: Same as (44)
 - b. Establish the RTO mode, and set the CH2 input coupling mode to GNd.
 - c. Establish the STORAGE mode, and adjust RV5252 so that the trace is positioned at the center of the CRT.
 - d. Establish the RTO mode again, and verify that the trace is positioned at the center of the CRT.
- AD1 EQ OFFSET (equivalent sample OFFSET) RV5203 (PEF-880) a. Set: Set to the state that the adjustment of 46 has finished.
 - b. Set the A TIME/DIV to 2 μ s/DIV.
 - c. Adjust RV5203 so that the trace is positioned at the center of the CRT.

Check of the frequency characteristics in the equivalent 48) sampling mode (no controls) (1) Overshoot a. Set: CH1 V MODE: CH1 VOLTS/DIV: 10 mV CH1 input coupling: DC (The AC/DC switch is pushed in.) $A = 0.1 \ \mu s$ A TIME/DIV: SOURCE OR X: CH1 (-)TRIGGER SLOPE: CH1 INPUT: Connect the 1 MHz square wave (Tr<1 ns) from the Tektronix PG-506 or equivalent to the instrument and adjust the PULSE AMPLITUDE control on the PG-506 so that the amplitude is 5 divisions on the CRT. ON (LED blinks, and the storage STORAGE: mode is established.)

x10 MAG:

ON

b. Adjust the TRIGGER LEVEL control so that the square wave is displayed on the CRT.

c. Verify that the overshoot is within ±4% (±0.2 divisions).

- (2) Rise time
- a. Set:

CH1 VOLTS/DIV: 10 mV

A TIME/DIV: A = 2ns

CH1 INPUT: Connect the 50 kHz sine wave from Tektronix SG-503 or equivalent to the instrument, and adjust the OUT-PUT AMPLITUDE on the SG-503 so that the amplitude is 6 divisions on the CRT. b. Set the A TIME/DIV switch to 50 ns/DIV.

- c. VC-6025: Set the output frequency of the SG-503 to 50 MHz, and verify that the amplitude is more than 4.2 divisions.
 - VC-6045: Set the output frequency of the SG-503 to 100 MHz, and verify that the amplitude is more than 4.2 divisions.

5. DETAILED CIRCUIT DESCRIPTION

5.1 VERTICAL CIRCUIT $(\sqrt{1}, \sqrt{2}, \sqrt{3})1/2, \sqrt{7}1/3, \sqrt{9}1/5, \sqrt{5}1/2)$

The detailed block diagram of this circuit is shown in Fig.5-1. The circuit description is made, based on the block diagram and the schematic diagrams $\langle 1 \rangle$, $\langle 2 \rangle$ and $\langle 3 \rangle$. This circuit consists of the CH1 vertical circuit and the CH2 vertical circuit. These circuit configurations are almost identical.

COUPLING

The CH1 SIG fed to J1 is routed to the CH1 INPUT COUPLING circuit, and the input-coupling modes are selected by switches S1 and S11 to AC, GND, or DC.

1st ATTENUATOR

The CH1 SIG is then fed to the CH1 1ST ATTN (attenuator), and its signal level is attenuated to 1/1, 1/10 or 1/100.

INPUT AMP

The attenuated CH1 SIG is fed to the CH1 INPUT AMP, and its impedance is converted (high input impedance and low output impedance).

The AC component of the CH1 SIG flows from C20 to TR25 to TR40 to TR41 to TR42, while the DC component flows from R21 to IC26 to TR28 to TR40 to TR41 to TR42.

IC26 is a DC amplifier. TR28 is a common-base transistor, and separates the AC component from the DC component to prevent them from being loaded to each other. Further, TR28 makes the load impedance of TR25 (FET) high and makes the gain of the FET 1.

When an input is zero volts, an output should also be zero volts. However, even if an input is zero volts, some offset voltage appears at the output of an actual DC amplifier.

CH1 DC BAL RV37 compensates for an offset voltage of IC26. CH1 DC GAIN RV30 changes the amount of the DC feedback, controls the DC gain, and matches the DC gain to the AC gain. Diodes D23, D25, and D26 protect the INPUT AMP against an excessive input voltage. The voltage gain of the INPUT AMP is 2.5 times but it is

The voltage gain of the INPUT AMP is 2.5 times, but it is switched to 6.25 times by switch S2-3 at the 2 mV/div range.

2nd ATTENUATOR

The output of the CH1 INPUT AMP is fed to the CH1 2ND ATTN, its signal level is attenuated to 1/1, 1/2, 1/4 or 1/10 by the setting position of the VOLTS/DIV switch. The output impedance is always 150 Ω .

PANEL STATUS

The PANEL STATUS (1) converts the settings of the VOLTS/DIV switch S2-1, the 1st ATTN switch S2-2 and the 2nd ATTN switch S2-4/S2-3 into the voltage values, and provides the MPU for the real time oscilloscope (RTO) with the setting of each switch via $\boxed{2}$.

The relationship between the overall gain from J1 to CH1 2ND ATTN and the setting position of the VOLTS/DIV switch is shown in Table 5-1.

Tal	ble	5-1
-----	-----	-----

VOLTS/ DIV	1ST ATTN	INPUT AMP Gain	2ND ATTN	Overall Gain	VOLTS/DIV x Overall Gain
2 mV	1	6.25(x2.5)	1	6.25	12.5 mV/div
5 mV	1	2.5	1	2.5	12.5 mV/div
10 mV	1	2.5	0.5(÷2)	1.25	12.5 mV/div
20 mV	1	2.5	0.25(÷4)	0.625	12.5 mV/div
50 mV	1	2.5	0.1(÷10)	0.25	12.5 mV/div
0.1 V	0.1(÷10)	2.5	0.5(÷2)	0.125	12.5 mV/div
0.2 V	0.1(÷10)	2.5	0.25(÷4)	0.0625	12.5 mV/div
0.5 V	0.1(÷10)	2.5	0.1(÷10)	0.025	12.5 mV/div
1 V	0.01(÷100)	2.5	0.5(÷2)	0.0125	12.5 mV/div
2 V	0.01(÷100)	2.5	0.25(÷4)	0.00625	12.5 mV/div
5 V	0.01(÷100)	2.5	0.1(÷10)	0.0025	12.5 mV/div

At the CAL position of the CH1 VAR control, R52 is shorted. At the fully CCW position, the output of the CH1 INPUT AMP becomes less than 1/2.5 times the output at the CAL mode. The information on the CAL or UNCAL status is also sent to the MPU for RTO. (For details, refer to Figs. 5-14 and 5-15.)

V PREAMP

The CH1 SIG from the CH1 2ND ATTN is fed to the CH1 V.PREAMP, where the signal is converted from the single-ended signal to the paraphase signal, and then fed to the DIODE GATE 1 at the next stage.

The DC voltage at the TR58 base is changed by CH1 POS RV1604 in the circuit $\langle 9 \rangle$, and the vertical position of the CH1 SIG is changed.

TRIGGER PICKOFF

A part of the CH1 SIG from the CH1 2ND ATTENUATOR is fed to the TRIGGER PICKOFF(1), and becomes the CH1 TRIG SIG. The time constant of the output impedance of the TRIGGER PICKOFF(1) is equal to that of the feedback impedance of the TRIGGER AMP in the next stage (Fig. 5-3). Therefore, the impedance ratio of the two circuits is always constant independent of frequency.

DIODE GATE

The DIODE GATE 1 is controlled by the $\overline{CH1}$ DSP signal from $\overline{7}$. When the $\overline{CH1}$ DSP signal is L, the CH1 SIG passes the DIODE GATE 1, and it is supplied to the DELAY LINE DRIVER at the next stage.

TR401 is a drive circuit of the DIODE GATE 1, and detects the operating state of CH1 (whether the CH1 SIG is in the state to be displayed or not).

TR407 is a stabilization circuit to prevent a shift of the DC level caused by the control switch. In other words, TR407 changes the current flowing in TR407 according to the operating states of CH1 and CH2 to maintain the DC voltages at points (a) and (b) constant. The CH2 SIG is fed to the DIODE GATE 2 via TR SW(1) or TR SW(2). The polarities of the input and output of TR SW(2) are opposite to those of TR SW(1).

When CH2 INVERT switch S1611 of $\langle 9 \rangle$ is switched to the INV side, the CH2 INV signal is pulled down by the resistor in invertor IC172, and turned to low. Then, each base of TR175 and TR176 goes high, and TR SW(2) (TR175 and TR176) turns to on. On the other hand, the TR SW(1) turns to off because the bases of and TR172 are low. Thus, the CH2 signalis fed TR171 to the 2 via TR SW(2), and the display polarity DIODE GATE is inverted.

DELAY LINE DRIVER

The signal is then supplied to the DELAY LINE DRIVER. Because this driver circuit is a common-emitter voltage feedback circuit, the impedance of the input and the output is low.

Flow of V SIG in RTO and DSO modes

The DELAY LINE output signal is routed to the RTO/DSO (digital storage oscilloscope) switch of $\langle 12 \rangle$ via 64 and 65. When RTO is selected, the DELAY LINE output is sent back to 67 and 68 and amplified by the V.AMP(1) consisting of TR501 and , TR502. GAIN RV505 adjusts the V. OUTPUT AMP so that its output is displayed corresponding to the deflection factor set by the VOLTS/DIV switch.

When DSO is selected, the DELAY LINE output is fed to the sample-and-hold circuit, the A/D circuit and the D/A circuit. Then the signal is routed to the V.AMP (2) as the waveform signal (Y component) or character signal (Y component) for DSO from 11 (9) via the DIFF AMP.

The DIFF $AMP(\langle 3 \rangle)$ is a circuit for converting the single-ended signal into the paraphase signal. Because the V.AMP(2) is a parallel feedback amplifier, the input impedance is small.

CHR-Y(CHST-Y) and A/B SEP BIAS signals

(1) RTO mode

When the horizontal display mode is other than the ALT sweep, approximately +1 volt is supplied. In the ALT sweep mode, the +1 volt (for A sweep) and the voltage (for B sweep) obtained by adding a certain voltage to the +1 volt are supplied alternately. The A/B SEP operations are displayed simultaneously for CH1 and CH2. At the timing to display characters on the CRT, the CHR Y

signal (voltage in the Y direction for each dot consisting characters or cursors) is supplied.

(2) DSO mode

The voltage in the Y direction (CHST-Y) for each dot of waveforms or characters (including cursors) in the DSO mode.

BWL (Band Width Limiter)

As the BWL circuit is provided between the V.AMP(2) and the V.OUTPUT AMP, more than 10 MHz for the VC-6025 and more than 20 MHz for the VC-6045 are attenuated under some conditions.

In the RTO mode, whether the signal is routed to the BWL circuit or not is determined by switch S1612.

The switch is marked "BW LIMIT 10 MHz" for the VC-6025 and "BW LIMIT 20 MHz" for the VC-6045. When this switch is pressed in the RTO mode, the BWL(1) for display and the BWL(2) for trigger become on simultaneously.

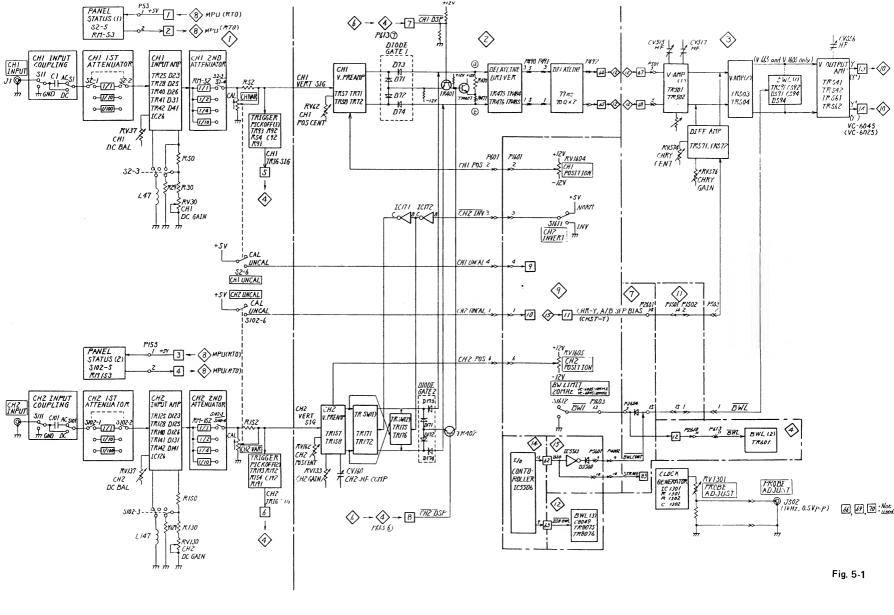
In the DSO mode, the DSO signal on pin 13 of IC5506 of 14 goes high, and the BWL(1) for display becomes on automatically. When the BWL(2) for trigger becomes on or not is determined by switch S1612. In the DSO mode, the output DSO BWL on pin 9 of IC5506 of 14 goes low only at 2 mV/DIV, and the BWL(3) of the sample-and-hold circuit becomes on. The BWL(3) attenuates more than 10 MHz for the VC-6025 and more than 20 MHz for the VC-6045.

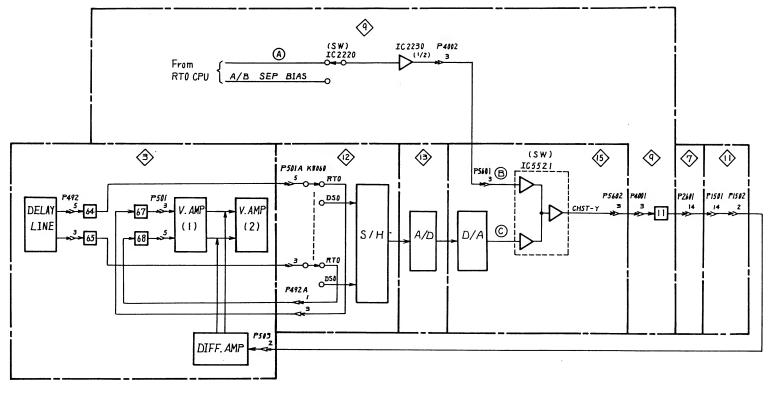
The signal from the V.AMP (2) is fed to the cascode-V.OUTPUT AMP, and amplified up to the voltage required for the vertical deflection.

5.2 CALIBRATOR (3 2/2)

For this circuit, refer to Fig.5-1.

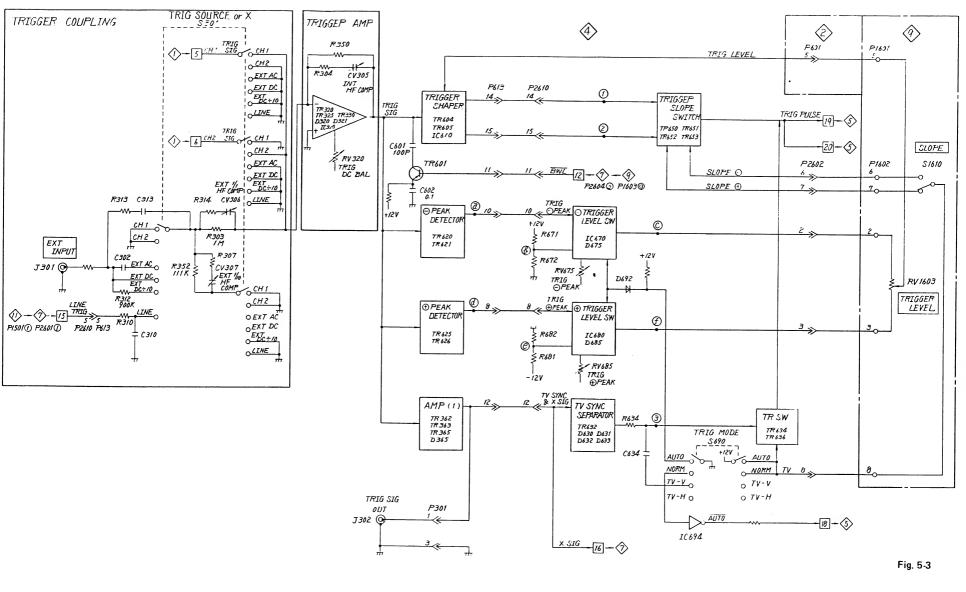
IC1301 is a clock generator, and its oscillation frequency is determined by R1301, R1302, and C1302. The 2 kHz frequency oscillated by R1301, R1302 and C1302 is counted down to 2:1 by IC1301, and a symmetrical 1 kHz square waveform is fed out from pin 4 of IC1301. The output level of IC1301 is adjusted by RV1303 so that the output from PROBE ADJUST J502 becomes 0.5 Vp-p.





- (A) Y component of characters (including cursors) in RTO mode
- (B) Y component of characters (including cursors) in RTO mode or A/B SEP BIAS
- © Y component of waveform or characters (including cursors) in RTO mode

Fig. 5-2



5.3 TRIGGER CIRCUIT (4 , 9 2/5)

The detailed block diagram of this circuit is shown in Fig. 5-3. TRIGGER SOURCE

The trigger-coupling modes selected by TRIG OR X SOURCE are CH1, CH2, AC, DC, DC \div 10, or LINE. The TRIG SIG is supplied from 5 in the CH1 mode, from 6 in the CH2 mode, from 15 in the LINE mode, and from EXT INPUT J301 in the other modes.

TRIGGER AMP

TRIG SIG from the TRIGGER COUPLING is fed to the TRIG The AMP and is amplified to the fixed signal level. The polarities at the input and output of TRIGGER AMP are opposite. The AC component of the TRIG SIG flows from TR320 to TR325 to TR330, while the DC component flows from R320 to IC320 to **TR325** to TR330. TRIG DC BAL RV320 adjusts the offset voltage of IC320, and the feedback impedance of the TRIGGER AMP consists of R350, R304, and CV305. For the TRIGGER AMP, refer to TRIGGER PICKOFF in 5.1 VERTICAL CIRCUIT. The TRIG SIG from the TRIGGER AMP is supplied to the TRIGGER SHAPER, (+) PEAK DETECTOR, (-) PEAK DETECTOR, and AMP(1).

The bandwidth of the TRIG SIG can be limited as appropriate. When the BW LIMIT switch S1612 (9) on the front panel is pressed, the BWL signal from 12 goes low, and switching transistor TR601 is turned on. Then the high frequency component of the TRIG SIG is bypassed to GND via C601 and C602, resulting in limiting the bandwidth. For the BWL, refer to 5.1 VERTICAL CIRCUIT.

TRIGGER SHAPER, PEAK DETECTOR and TRIG MODE

The TRIGGER SHAPER is a comparator with a hysteresis characteristics, and feeds out the trigger pulses to (1) and (2) by comparing the TRIG LEVEL set by TRIG LEVEL RV1603 in (9) with the TRIG SIG. The polarities of the trigger pulses are opposite each other.

The (+) PEAK voltage of the TRIG SIG is fed to (a) by the (+) PEAK DETECTOR, and the (-) PEAK voltage is fed to (d) by the (-) PEAK DETECTOR. Therefore, the voltages at (a) and (d) are changed by the minimum and maximum voltages of the TRIG SIG. On the other hand, the positive fixed voltage is generated at (b), and the negative fixed voltage is generated at (e).

The voltage at (a) or (b) is fed to (c) , and the voltage at (d) or (e) is fed to (f). The supplied voltages are determined by TRIG MODE S690 in (3). When the TRIG MODE is at AUTO, the voltage at (a) (the positive peak voltage of the TRIG SIG) is fed to (c), and the voltage at (d) (the negative peak voltage of the TRIG SIG) is fed to (f). Therefore, it is possible to correspond the variable range of TRIG LEVEL RV1603 in (9) with the amplitude of the trigger signal, and it is easy to set the trigger level.

When the TRIG MODE is at NORM, TV-V, or TV-H, the voltage at b (the positive fixed voltage not affected by the minimum and maximum voltages of the TRIG SIG) is fed to c, and the voltage at e (the negative fixed voltage) is fed to f. Therefore, the variable range of TRIG LEVEL RV1603 in 9 is constant independent of the amplitude of the trigger signal. Information on the TRIG MODE selection is transmitted to the circuit 5 from 18 via INVERTOR TR694. AMP(1) is a negative feedback amplifier. The polarity of the

TRIG SIG is inverted here. The inverted TRIG SIG is sent to the TV SYNC SEPARATOR, $\langle 7 \rangle$, and TRIG SIG OUT J302.

SYNC SEPARATOR and TRIG MODE

In the SYNC SEPARATOR, the SYNC component of the TRIG SIG is separated regardless of the horizontal and vertical sync signals.

When the TRIG MODE is at AUTO or NORM, TR636 of TR SW(1) is on, the base of TR634 is grounded, and the TR SW(2) turns off. Therefore, the output of the TV SYNC SEPARATOR can not pass through the TR SW(2).

When the TRIG MODE is at TV-V or TV-H, the TR SW(1) is off, and the TR SW(2) turns on. Therefore, the output of the TV SYNC SEPARATOR can pass through the TR SW(2).

When the TRIG MODE is at TV-V, one side of C634 is grounded, and R634 and C634 compose an integrating circuit. As a result, the H SYNC is interrupted, and only the V.SYNC passes through the TR SW(2).

TRIG SLOPE SWITCH

The TRIGGER SLOPE SWITCH consists of the two current switch circuits. One consists of TR650 and TR651, and the other consists of TR652 and TR653.

When TRIG MODE S690 is at AUTO or NORM, +12 V is supplied to SLOPE S1610. When SLOPE S1610 is switched to the (+) SLOPE side, +12 V is supplied to the current switch circuit consisting of TR650 and TR651, and the voltage at (1) is fed out from the TRIGGER SLOPE SWITCH.

When the TRIG MODE is at AUTO or NORM and SLOPE S1610 is switched to \bigcirc SLOPE side, +12 V is supplied to the current switch circuit consisting of TR652 and TR653, and the voltage at \bigcirc is fed out from the TRIGGER SLOPE SWITCH. When the TRIG MODE is switched to TV-V or TV-H, +12 V is not supplied to any current switch circuit, and the voltage at neither \bigcirc nor \bigcirc is fed out from the TRIGGER SLOPE SWITCH.

In this case, as stated above, the voltage at (3) (H.SYNC or V.SYNC) is fed out from 19 via the TR SW(2). Thus, one of the signals (1), (2), and (3) is fed out from 19 as a TRIG PULSE by the combination of TRIG MODE S690 and SLOPE S1610.

5.4 SWEEP CYCLE $(\langle 5 \rangle)$

This circuit is provided to perform a cycle sweep, which is one of the major features of this oscilloscope. Since the sweep circuit and the hold-off circuit are operated independently, the cycle time (= sweep time + hold-off time) can be fixed. In other words, when the TRIGGER LOCK control on the front panel is pressed (the cycle lock on mode), the cycle time is fixed by the MPU for the RTO and a stable trigger is obtained regardless of the sweep time (TIME/DIV range).

The main operation of this circuit is described below, referring to the simplified circuit diagram shown in Fig. 5-4.

- (1) The sweep state (the trigger sweep or the free-running sweep) is determined by the state of the signal on pin 2 of IC661 (3/4). In the trigger sweep mode, pin 3 goes high and D665 turns to off because pin 2 is low.
- (2) When the hold-off voltage \overline{HOLD} OFF goes low, DELAY GATE (CYCLE GATE) IC660 (2/2) is reset, and $\overline{Q2}$ goes high.
- (3) When $\overline{Q2}$ goes high, D664 is off, and the DLY GATE signal goes high.
- (4) Thus, switching transistor TR2010 turns on, and the gate voltage of BUFFER TR2060 is set to the starting level of the DELAY RAMP.
- (5) When the hold-off period finishes, the HOLD OFF changes from low to high. In other words, IC660 (2/2) is released from the reset state and is in the wait state.
- (6) When the TRIG PULSE is fed to T2 from 20, $\overline{Q2}$ changes from high to low during the rising edge of the TRIG PULSE.

- (7) When $\overline{Q2}$ goes low, D664 is on, and the DLY GATE signal is low.
- Then TR2010 turns to off, delay capacitor $C_{DI,Y}$ (C2012 // (8) C2013) starts to be charged, and the gate voltage of BUFFER TR2060 starts to increase. The charging current is supplied from the delay current source, and the current value is changeable by the TIME/DIV setting. When the TIME/DIV setting value is set, the constant charging current flows in C_{DLY}. As a result, the gate voltage of TR2060 increases linearly. The delay current signal from 26 is an analog voltage to determine the delay current. The voltage is held by C2017, is applied to pin 10 of IC2040 (3/4) through the and filter consisting of R2015 and C2015.
- Portion of the output of BUFFER TR2060 is sent to (9) COMPARATOR IC2050 (2/2) as a DELAY RAMP signal. In this comparator, the output levels of ACTIVE FILTER IC2040 (1/4) and the DELAY RAMP signal are compared. When the DELAY RAMP signal level exceeds the output level of the ACTIVE FILTER, the output of the COMPARATOR goes high. Accordingly, the DLY TRIG signal goes low. In the B sweep mode, the sweep starts after the predetermined delay time from the trigger point. Either the DLY REF signal from 37 or the DLY PRESET signal from 38 is fed to the ACTIVE The DLY REF signal is fed to the ACTIVE FILTER in FILTER. the normal delay mode, and the DLY PRESET signal is fed to the ACTIVE FILTER in the automatic calibration mode. The DLY REF signal is the voltage corresponding to the delay time set by the controls on the front panel. The other portion of the output of BUFFER TR2060 is fed to COMPARATOR TR2063, and used to detect the maximum voltage

of the DELAY RAMP signal. Normally, the output of COMPARATOR TR2063 is high, the output (\overline{Q}) of RS LATCH IC2052 3/3 is low, and the output (HOLD OFF) of IC2052 2/3 is high. When the DELAY RAMP signal reaches the maximum value, the output of COMPARATOR TR2063 goes low (because TR2063 turns to on). Therefore, the RS LATCH is reset, \overline{Q} goes high, and the HOLD OFF signal goes low.

- (10) As a result, DELAY GATE (CYCLE GATE) IC660 2/2 is reset, $\overline{Q2}$ signal goes high. This state is the same as that of step (3). Then D664 turns to off, TR2010 turns to on, and the gate voltage of BUFFER TR2060 is set to the start level of the DELAY RAMP. Moreover, the output of COMPARA-TOR TR2063 returns to high.
- (11) Next, the circuit related to the HOLD OFF RAMP signal is described below. When the DLY GATE is low, TR2040 is on, and the collector voltage of TR2045 remains at the start level of the HOLD OFF RAMP signal.
- (12) The integration of the DELAY RAMP signal finishes before the output of TR2063 described in step (10) goes high, and TR2040 changes from on to off. At this time, the integration of the HOLD OFF RAMP starts.
- (13) TR2040 turns to off, HOLD OFF CAPACITOR C_{HO} (C2042 // C2043) begins to be charged, and the collector voltage of TR2045 begins to increase. The charging current is supplied from the HOLD OFF CURRENT SOURCE. This current value is changeable by the TIME/DIV setting value. When the TIME/DIV setting value is set, the constant charging current begins to flow, and the collector voltage of TR2045 increases linearly.

- (14) The collector voltage of TR2045 and the VAR H/O voltage fed via VOLTAGE FOLLOWER IC2040 (4/4) are compared by COMPARATOR IC2050 (1/2) in the next stage. The VAR H/O voltage corresponds to the setting value of the VARIABLES and HOLD OFF controls on the front panel.
- (15) When the HOLD OFF RAMP voltage (the collector voltage of TR2045) exceeds the VAR H/O voltage, the output of COMPARATOR IC2050 (1/2) goes low.
- (16) Thus, RS LATCH IC2052 (3/3) is in the set state, and Q goes low.
- (17) As a result, HOLD OFF (the output of IC2052 2/3) goes high and the period of the holdoff finishes.

In case of a single sweep

- (a) The maximum VAR H/O voltage is fed to 36 .
- (b) The upper limit value of the HOLD OFF RAMP voltage is clamped to the voltage lower than the VAR H/O voltage by CLAMP TR2080.

Thus, "L" is not output from COMPARATOR IC2050(1/2), and the hold-off state continues after swept once.

When the reset switch is pressed, the VAR H/O voltage lower than the upper limit of the HOLD OFF RAMP voltage is fed from 36 . As a result, the COMPARATOR output goes low, resulting in releasing the hold-off state.

When the single switch is pressed thereafter, the above (a) and (b) state is regained.

(i) A SWEEP

- (a) Since the A signal from 25 is low, the output from pin 11 of IC661 (1/4) is high, and TR661 is on. Therefore, the DLY TRIG signal cannot pass the differentiation circuit consisting of C669 and R669A in the next stage and S1 of SWP GATE IC660 (1/2)remains high. This is because only the rapid changing component of the signal can pass the differentiation circuit. In other words, in the A SWEEP the route of the DLY TRIG signal is not used.
- (b) Moreover, since the output from pin 11 of IC661 (1/4) is high, D660 turns to off, and pin 9 of IC659 goes high. In case of the trigger sweep, pin 3 of IC661 (3/4) is also high, and D661 is off.
- (c) When $\overline{Q2}$ changes from high to low under the above state, the output from pin 8 of IC659 changes from low to high. That is, when T1 of SWEEP GATE IC660(1/2) changes from low to high, Q1 changes from low to high, and the SWP GATE signal from $\overline{Q1}$ changes from high to low. Thus, the sweep begins.

(ii) B SWEEP

- (a) Since the \overline{A} signal from 25 is high, the output from pin 11 of IC661 (1/4) goes low.
- (b) Therefore, D660 is on, and pin 9 of IC659 goes low. The output of pin 8 remains high independent of the state of pin 10 of IC659. In case of the B SWEEP the route of S1 is not used.
- (c) On the other hand, the output from pin 11 of IC661 (1/4) is low, and TR661 becomes off.
- (d) Therefore, when the DLY TRIG signal changes from high to low, the change is applied to terminal S of SWEEP GATE IC660 (1/2) through the differentiation circuit.

(e) As a result, IC660 (1/2) turns to the set state, Q1 changes from low to high , and Q1 changes from high to low. Thus, the B SWEEP begins.

The DLY ADJUST signal from 21 is the signal for the automatic calibration of the delay time. Though the delay time is controlled by a screwdriver adjustment in conventional oscilloscopes, in this oscilloscope, the delay time is calibrated automatically by the built-in MPU for the RTO when the power switch is turned on.

(iii) Relation with STORAGE

In the STORAGE mode, the RTO/STR from 74 goes high, and the SWP GATE on pin 13 of IC659 passes through IC659, resulting in the GATE signal. In the RTO mode, the output signal from IC659 is always high, and the SWP GATE can not pass through IC659. The sweep output of 6 is supplied to 71. The SWEEP signal from 72 and the GATE signal from 73 are supplied to the circuit 13, and controls the sampling operation in the storage mode.

AUTO GATE circuit

- (A) NORM mode (trigger sweep) The AUTO signal from 18 is high, and TR660 is on. Pin 2 of IC661 (3/4) goes low, and pin 3 goes high. Therefore, D665 turns to off, the AUTO GATE circuit does not function in the NORM mode.
- (B) Auto mode (including TV-V and TV-H) The AUTO signal from 18 goes low. There are two kinds of sweep in the AUTO mode: the trigger sweep and the freerunning sweep.

- (a) Trigger sweep in AUTO (including TV-V and TV-H)
 - When the TRIG PULSE is supplied to T2, Q2 changes from low to high during the rising edge of the pulse.
 - 2 When Q2 goes high, TR660 turns to on, C664 is shorted, and pin 2 of IC661 (3/4) remains low.
 - (3) When the DELAY RAMP signal voltage reaches the maximum, the HOLD OFF signal is low, and the holdoff period begins.
 - When the HOLD OFF signal goes low, Q2 changes from high to low, and TR660 turns to off. On the other hand, D663 turns to on, the anode side of D662 goes low, and D662 becomes off. Therefore, C664 is not charged. Pin 2 of IC661 (3/4) remains low.
 - 5 When the hold-off period finishes, the HOLD OFF changes from low to high, D663 turns to off. As the anode side of D663 goes high, D662 turns to on, and C664 begins to be charged.
- (6) As a result, the voltage on pin 2 of IC661 (3/4) increases gradually. However, the trigger pulse is repeatedly fed to pin 2 of IC661 (3/4) before the voltage reaches the threshold level, and the low level, namely the trigger sweep state, is maintained.
 (b) Free-running sweep in AUTO (including TV-V and TV-H)

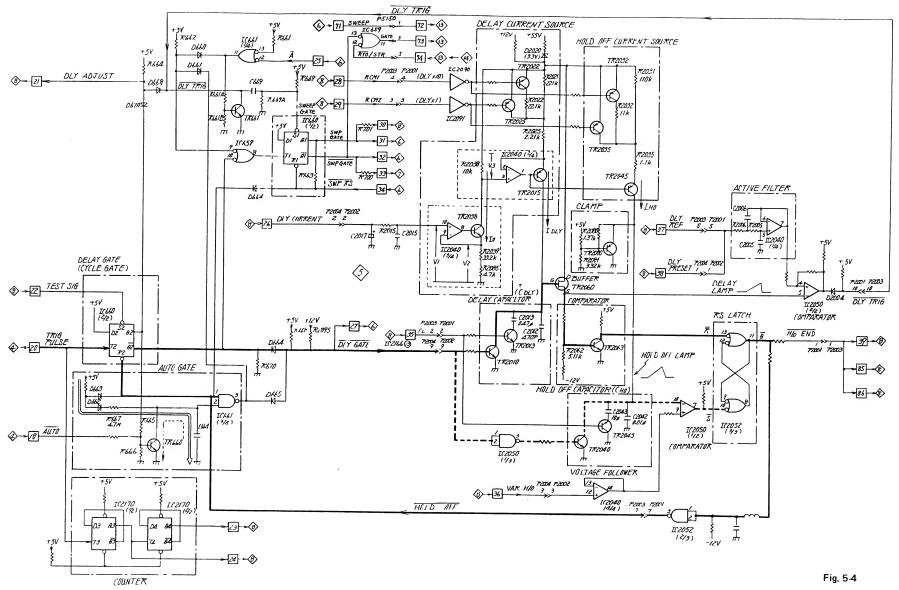
TRIG PULSE is not fed when the voltage on pin If 2 of IC661 (3/4) reaches the threshold level in the above description (a) (6) (even when pin 2 changes from low to high), the free-running sweep begins. In other words, when pin 2 goes high, pin 3 goes low, and D661 and D665 turn to on. When D661 is on, pin 9 of IC659 goes low, pin 8 goes high, and the sweep begins. When D665 turns to on, the DLY GATE signal goes low, and the DELAY RAMP signal is generated.

COUNTER circuit IC2170 (1/2, 2/2)

When the TRIG PULSE is fed to T3, the divided-by-two pulse is fed out from Q3, and the divided-by-four pulse is fed out from Q4. These pulse are sent to the MPU for the RTO and used to count the frequency of the trigger pulse. The waveform of 1.6 to 4 cycles is displayed on the CRT in the AUTO range mode.

There are two reasons for using the divider circuits. One reason is to avoid routing the signal at a high frequency. (It must be noted that the pulse of max. 10 MHz is fed to T3). The other reason is why the clock frequency of the counter built in the MPU for the TRO is limited. (The clock frequency of the counter is 1 MHz.)

The number of trigger is counted by using the pulse from $\boxed{24}$ for a slow waveform and the pulse from $\boxed{23}$ for a fast waveform.



5.5 SWEEP (6 1/2)

The detailed block diagram of this circuit is shown in Fig. 5-5. When the sweep begins, the SWP GATE signal entered 32 at changes from high to low, and the SWP GATE signal entered at 31 changes from low to high. Accordingly, diodes D710, D711, and D712 turn to off. The TIMING CAPACITOR (C $_{
m T}$) is provided between the input and the output of the INVERTING AMP consisting of TR710, TR712, and TR714 to form an miller integrator. $C_{
m T}$ is determined by C710 // C711 or C710 // C711 // C715. The integration current $I_{\mathrm{T}}^{}$ is determined by the input voltage of IC730 (1/2) and the timing resistors ($R_{
m T}$), which are determined by the TIME/DIV setting. The value of C_{T} is determined by C710 // C711 or C710 // C711 // C715. The value of R_T is determined by R740, R740 // R741, R740 // R743 or R740 // R745. When diodes D710, D711, and D712 turn to off, the integration current I_{T} begins to flow to the TIMING CAPACITOR C $_{\mathrm{T}}$, and the voltage of C_{T} begins to increase linearly corresponding to I $_{\mathrm{T}}.$

The output voltage of the INVERTING AMP is fed out from 50 as the SWP OUT signal via ANALOG SW2 IC717. Part of the output voltage of the INVERTING AMP is fed to voltage comparator TR723 via ANALOG SW2 IC717, and the maximum voltage of the SWP OUT signal is determined by comparing the output voltage of the INVERTING AMP with the base voltage of TR723. When **TR723** detects the maximum voltage, its collector voltage turns to low, and the SWP RS signals fed from 34 and 49 also turn to The $\overline{SWP RS}$ signal is applied to FF IC660(1/2) (13) low. shown in $\langle 5
angle$, and turns the output of the SWP GATE to high. When the SWP GATE goes high and the SWP GATE goes low, diodes D710, D711, and D712 turn to on. The input and the output of the INVERTING are thus shorted, and the TIMING CAPACITOR AMP C_{T} discharges rapidly. As a result, the output voltage of the INVERTING AMP

falls down to the voltage at the beginning of the sweep, voltage comparator TR723 turns to off, and the collector voltage of TR723 is reset to high.

The CS A DATA signal entered at 44 is a DC voltage (analog value) corresponding to the A sweep, and the CS B DATA signal entered at 45 is a DC voltage (analog value) corresponding to the B sweep. The CS A and CS B DATA signals are changed by the TIME/DIV setting, and accordingly, the voltage V_T of the V_T/I_O CONVERTER is changed. The TIME/DIV setting is changed to 1:2:5 by changing the voltage V_T . The figures of the TIME/DIV setting value are determined by changing the value of the timing resistor R_T to 1:10:100:1000.

The Q_E output (\overline{A}) of SHIFT REGISTER IC2165 controls ANALOG SW1 IC717 via IC738. The CS A DATA signal and the CS B DATA signal are supplied to the V_T/I_O CONVERTER in the A sweep mode and in the B sweep mode, respectively. V_T is a voltage corresponding to the CS A DATA signal or the CS B DATA signal, and the current I_O corresponding to V_T flows across R732. The resulting voltage V_O is fed to the V_O/I_T CONVERTER and the output current I_T corresponding to V_O flows to the TIMING RESISTOR R_T . The V_T/I_T CONVERTER consists of the V_T/I_O CONVERTER and the V_O/I_T CONVERTER, and the current I_T corresponding to the CS A DATA signal or the CS B DATA signal is obtained. Since I_T is fed to the miller integrator, the SWP OUT signal corresponding to the CS A DATA signal or the CS B DATA signal is obtained.

 R_{T1} , R_{T2} , and R_{T3} fed from Q_B , Q_C , and Q_D of SHIFT REGISTER IC2165 are control signals to switch the timing resistor R_T . R_{T1} , R_{T2} , and R_{T3} are supplied to switching transistors TR745, TR743 and TR741 via LEVEL SHIFT TR750, TR751, and TR752, respectively, and the value of R_T is determined. Only the A sweep is provided with the SWP VAR function, and the voltage value of the CS A DATA signal is changed continuously by the MPU for the RTO.

IC2165 is an 8-bit shift register having serial inputs and parallel outputs. The 8-bit shift register and the latch are packed onto a single chip. The S DATA signal fed to the SER is shifted to the register bit by bit during every rising edge of the shift register clock S CLK2 signal fed to the SRCK.

The 8-bit data in the register is transferred simultaneously to the latch circuit during the rising edge of the register clock pulse entered at RCK and the latch data is updated. (While the S DATA signal is being acquired, Q_A to Q_H are being held in the previous state and the data on Q_A to Q_H is updated during the rising edge of RCK.) The shift register and the latch circuit (storage register) have the individual clear signals (shift register clear SRCLR signal and register clear RCLR signal).

The clear signals are synchronized with the clock pulse when they are high.

The S DATA signal from 42 switches the TIME/DIV setting and the vertical channel. The clock pulse S CLK2 is fed from 43only when the content of the S DATA is changed.

The S CLK2 pulse is generated by PC2 and PC6 pulses fed out from IC3101 of the MPU for the RTO shown in $\langle 8 \rangle$. PC2 is a clock pulse being fed out continuously. PC6 is a clock enable signal and controls the clock pulse P2. The passage of the clock pulse through the gate circuit (IC2107 of $\langle 8 \rangle$) is controlled by the PC6 signal. The clock pulse passing the gate circuit (IC2107 shown in $\langle 8 \rangle$) is an S CLK2 pulse.

The route of a register clock pulse fed to the RCK terminal (pin 12) of SHIFT REGISTER IC2165 is different in the normal sweep mode and in the non-sweep mode (mainly in the X-Y mode).

(1) When the sweep is performed

When the DLY GATE signal from 27 changes from low to high, the register clock pulse fed to the RCK terminal changes from low to high, and the 8-bit data in the register is transferred simultaneously to the latch circuit during the rising edge of the register clock pulse. Strictly speaking, since the DLY GATE signal passes through the differentiation circuit consisting of C2167 and R2167, and gate circuit IC2162 (2/4), the register clock pulse changes from low to high after the DLY GATE signal has changed from low high. This is because the latch data is updated when the hold-off period begins completely.

The PC6 signal from 40 changes the state of pin 5 of IC2162 (2/4), and controls the transmission of the change of the DLY GATE signal to the RCK terminal. When the updating of the latch data is prohibited, namely when a new S DATA is being sent, PC6 from 40 is high. Therefore, pin 5 of IC2164 (2/4) goes low, and the change of the DLY GATE signal cannot pass through the gate circuit IC2162 (2/4). When all the data of 8-bit S DATA is shifted to the shift register, and the sweep is finished, data is transferred from the shift register to the latch circuit.

(2) When the sweep is not performed (mainly in the X-Y mode) The MPU for the RTO controls the transmission of the latch data directly. When the data is updated, a negative pulse is fed from 41 The output of $Q_{\rm H}$ is sent to the MPU for the RTO (IC3101) in (8) via [47] , and informs the microcomputer of the latch state. The S DATA fed to $Q_{H'}$ is fed to the front panel board via 48 . The LED's (D1601, D1602, and D1605 to D1611 in $\langle 9 \rangle$) on the panel are blinked by this output of Q_H. TR708 and TR709 are switching transistors. When the TIME/DIV switch is set to 0.5 ms or 0.2 ms, the Q_A and Q_B outputs of SHIFT REGISTER IC2165 are low and high respec-Thus, R703 is TR708 and TR709 become on. tively, and shorted, and the current flowing across R703A increases. As a result, the reset duration of the sweep waveform can be made short resulting in increasing the display ratio, and a brighter waveform can be observed.

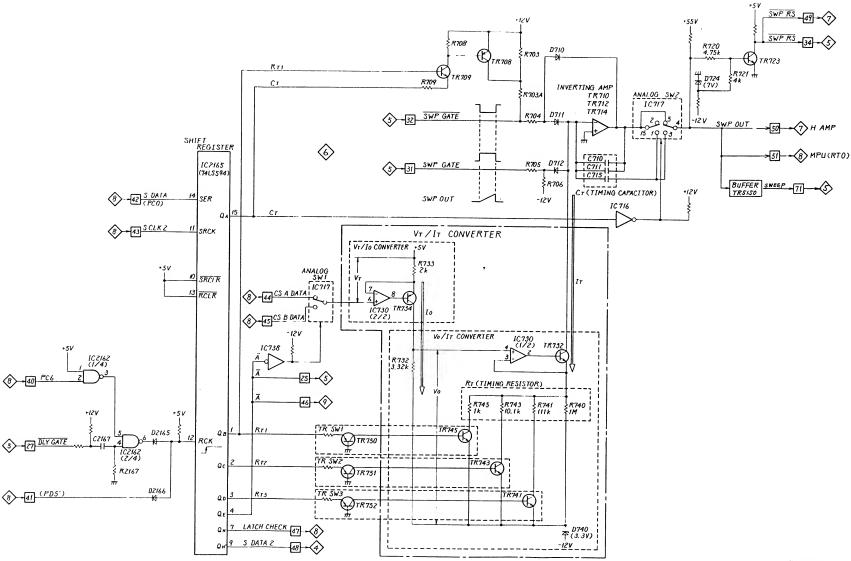


Fig. 5-5

5.6 H AMP (<7> 2/3, <9> 3/5)

Fig. 5-6 is the detailed block diagram of this circuit. Normally the TR SW (1) circuit is not activated, and the SWP OUT signal from 50 is applied to the DIFF AMP(1) circuit via the AMP (1) circuit. In the X-Y mode, the $\overline{X-Y}$ signal from 52 goes L, so that TR811 turns off and TR812 turns on. Therefore, the TR SW (1) circuit is activated, and the X-SIG from 16 is applied to the DIFF AMP(1) circuit via the AMP(1) circuit. the other hand, the H POS signal from 53is set to the optimum DC voltage by H POS START RV807, and is applied to the DIFF AMP(1) circuit via the AMP(2) circuit.

The DIFF AMP(1) circuit is activated in the waveform display mode, and the DIFF AMP(2) circuit is activated in the dot display mode. When I_1 or I_2 flows, the DIFF AMP(1) circuit is activated. When I_3 flows, the DIFF AMP(2) circuit is activated. Either of I_1 , I_2 or I_3 is always flowing. I_1 flows in the x1 mode, I_2 in the x10 mode, and I_3 in the dot display mode.

The selection of I_1 , I_2 or I_3 is controlled by the $\overline{X1}$ signal from 54 and the DOT EN signal from 56.

state of the $\overline{X1}$ signal is determined by DPDT switch The (x10 MAG) S1605 in $\langle 9 \rangle$. One switching circuit (pins 4, 5, and 6) of S1605 controls the CURRENT SW(1) directly. The other switching circuit (pins 1, 2, and 3) informs the setting state (x1 or x10) of the MPU for the RTO by changing the output voltage AN0 of D/A(2) RM1601. Pressing the ALT and B switches simultane ously results in the X-Y mode, and pin 4 of S1605 is Therefore, in the X-Y mode, even if grounded. the x10 MAG switch is set to the x10 side, the switch is forced to return to the x1 mode. The states of the ALT and B switches are informed of the MPU for the RTO by the output voltage AN2 of D/A(1) RM1603.

For the following description, refer to the schematic diagram $\langle 7 \rangle$.

D841 and D842 are switching diodes, and change the current flow in the DIFF AMP(1) circuit according to the x1 or x10 mode. Both diodes turn off in the x1 mode, and on in the x10 mode. In the waveform display mode, the output of the DIFF AMP(1) circuit is applied to the DIFF AMP(3) circuit.

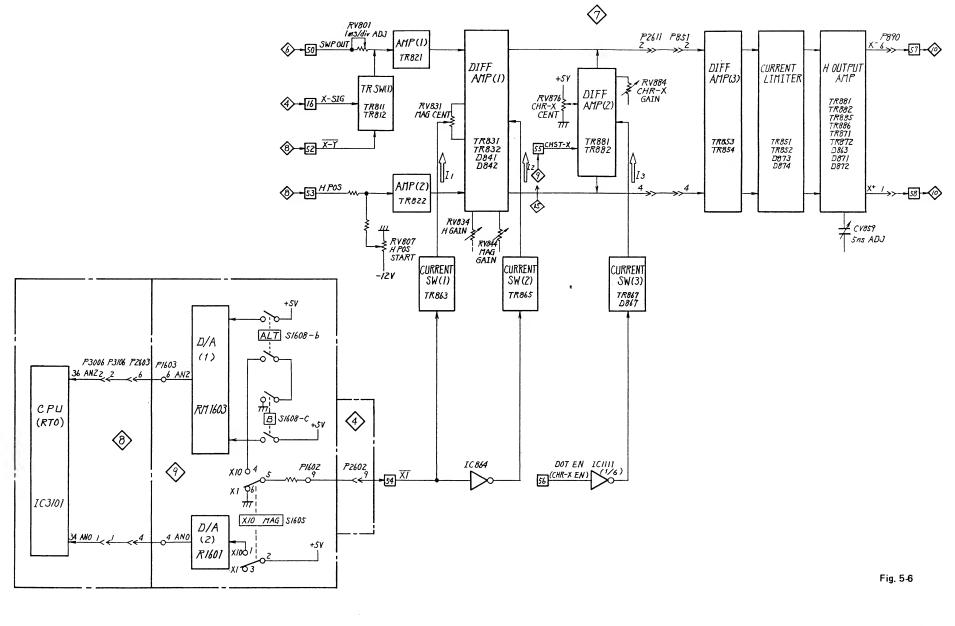
In the dot display mode, the output of the DIFF AMP(2) circuit is applied to the DIFF AMP(3) circuit.

The DIFF AMP(3) circuit employs a common-base circuit, and the low impedance input and the high impedance output are realized. The output of the DIF AMP(3) circuit is sent to the CURRENT LIMITER circuit consisting of the common-base DIFF AMP circuit (TR851 and TR852) and the diodes (D873 and D874). This CURRENT LIMITER prevents the H OUTPUT AMP circuit from being driven up to a saturation field.

The output signal current of TR851 is amplified by emitter follower stage TR881 and common-emitter stage TR885. The amplified output is fed back to the input through R857, R855, C857, and C855. The feedback amount at high frequency is adjusted by CV859 to optimize the linearity at the 5 ns/div sweep.

TR871 is an active load of TR885. The AC component is applied to the base of TR871 through C883 so that the supply current increases when the output voltage changes to the positive at a high speed.

The operation of the circuits following TR852 is identical with the above operation except for signal polarities.



5.7 UNBLANKING & Z-AXIS AMP ($\sqrt{7}$ 3/3, $\sqrt{9}$ 4/5, $\sqrt{10}$ 1/2)

Description on the UNBLANKING circuit and the Z-AXIS AMP circuit follows. Refer to Figs. 5-7 and 5-8.

UNBLANKING circuit

The UNBLANKING circuit consists of two functional blocks. One consists of IC1101 1/3, IC1101 3/3 and D1113 and controls a waveform display, and the other consists of IC1121 3/4 and D1114 and controls the readout character display. The intensity of the displayed waveform is controlled by the INTEN control and that of the readout (characters or cursors) by the READOUT INTEN control.

The waveform display and the readout display (characters or cursors) are performed by the time division.

Like the X-axis circuit and the Y-axis circuit, the UNBLANKING circuit in the Z-axis circuit is switched according to the time division. In other words, either of the two functional blocks (the UNBL and CHR Z signals) of the UNBLANKING circuit is selected by the DOT EN signal or the DOT EN signal according to the kind of the requested display, the waveform or the dots (characters of cursors).

To effect or not blanking of the waveform and the dots (characters or cursors) is controlled by the UNBL signal and the $\overline{CHR~Z}$ signal, respectively. When the waveform is displayed, the \overline{UNBL} signal is low, and the $\overline{CHR~Z}$ signal is high.

Since the emitter voltage of TR901 is always zero volts, D1113 is on, and D1114 is off. When the dots (characters or cursors) are displayed, the $\overline{\text{UNBL}}$ signal is high, and the $\overline{\text{CHR Z}}$ is low. Therefore, D1113 is off, and D1114 is on.

When the sweep begins and the SWP GATE signal from 33 goes low or the $\overline{X-Y}$ signal from 60 goes low in the X-Y mode, the

UNBL signal fed out from pin 8 of IC1101 (3/3) goes low, resulting in the waveform display state.

When the CHR EN from 76 goes high to display characters, or the CUR EN signal low from 59 goes low to display cursors, the DOT EN signal is fed out from pin 11 of IC1121 (4/4), and resulting in the dot display state.

The waveform becomes the blanking state (UNBL=H) in the following cases (1) to (4).

- (1) When the sweep finishes, and the SWP RS signal from 49 goes low.
- (2) While the MPU for the RTO are operating In this case, D1101 or D1105 turns on.
- (3) When the switching part needs to be blanked In this case, D1102 turns on.
- (4) Dot display

In this case, D1103 and D1104 turn on.

The H AMP is changed by the DOT EN signal (corresponding to the the CHR-X EN signal) fed out from 56, and the V AMP is changed by the DOT EN signal (corresponding to the CHR-Y EN signal) fed out from 61.

In the DSO mode, the STORAGE signal fed from 83 goes high and each switch of SELECTOR IC 4001 is switched to the B side. As a result, the STR-Z signal is fed out from 1Y, and 2Y becomes in the high state.

The 2Y output enters CURRENT SW(3) of $\langle 7 \rangle$ via 56, and allows I3 to flow, resulting in operating DIFF AMP (2). (Fig. 5-6) I1 and I2 do not flow, and DIFF AMP (1) does not work, Thus, in any case of waveforms, characters and cursors the X-direction signal is fed out via DIFF AMP (2) in the DSO mode.

The DOT EN signal from 61 controls the switching of ANALOG SWITCH IC2220 of 9. (Fig. 5-13) In the RTO mode, two kinds of blanking, waveforms and dots (characters or cursors), are

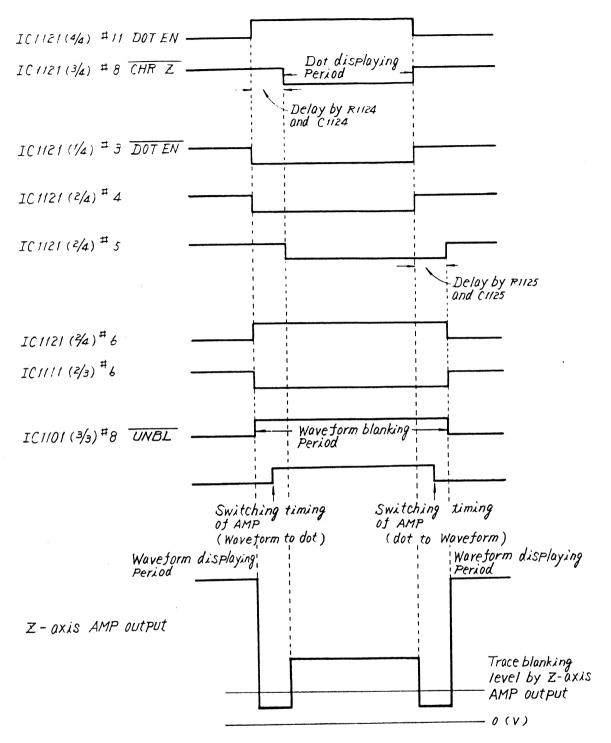
controlled. In the DSO mode, the blanking of dots (waveforms, characters and cursors) is controlled by the $\overline{\text{STR Z}}$ signal from $\boxed{82}$. In this case, the caracter generator circuit in the RTO mode is stopped by the MPU for the RTO. (The CHR Z signal is high.)

Z-AXIS AMP

This circuit consists of the current limiter (TR901 and D901) and the feedback AMP (TR906, TR910, and TR912). There are two input channels to this AMP. One is the waveform display channel of D1113, and the other is the dot display channel of D1114. These channels are selected by the DOT EN signal fed out from pin 11 of IC1121 (4/4). In either case, the current from TR901 emitter increases, the intensity of the CRT increases. The change of the input current applied to TR901 emitter is not transmitted to the collector, but the change is not transmitted to TR906 by D901. Therefore, the output voltage of the Z.AXIS AMP is controlled so that it is not lower than approx. 5 V.

When the current of TR901 (from the emitter) increases, the current across D901 increases. Therefore, the base voltage of TR906 decreases. As a result, the base voltage of TR912 decreases, and the output voltage of the Z-AXIS AMP becomes more positive. This output is connected with the electrode G1 for the beam control of the CRT. So when the output voltage of the Z.

AXIS AMP becomes further positive, the intensity increases accordingly.



Note 1 : The above waveforms are synchronous each other.

Note 2; The unblanking waveform in each sweep and the above waveforms are asynchronous.

Fig. 5-7

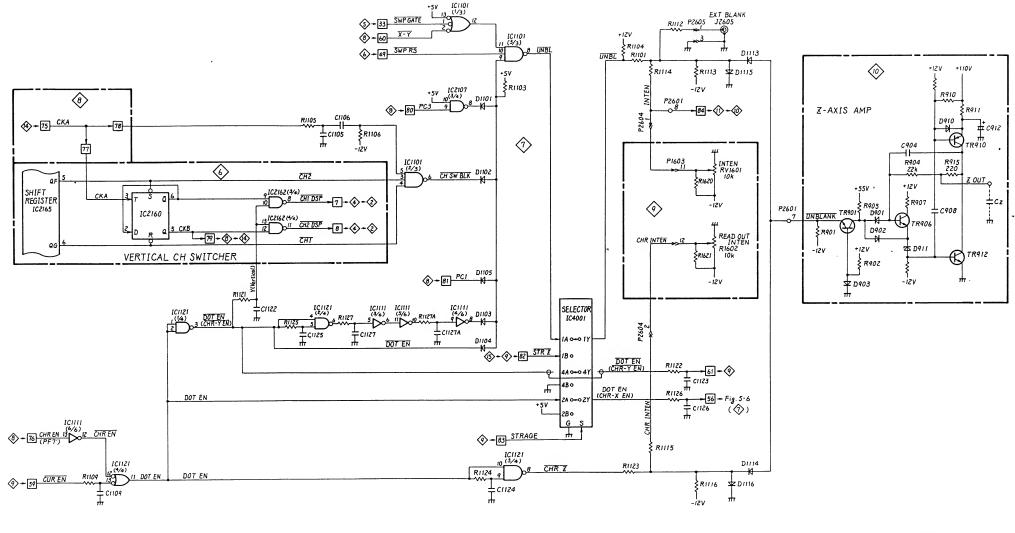


Fig. 5-8

5.8 VERTICAL CH SWITCHER ($\langle 6 \rangle$ 2/2)

Refer to Fig. 5-6 and Table 5-2.

The displayed channel is determined by the output signals CH1 $\overrightarrow{\text{DSP}}$ and $\overrightarrow{\text{CH2}}$ $\overrightarrow{\text{DSP}}$. The state of these output signals are determined by the $\overrightarrow{\text{CH1}}$, the $\overrightarrow{\text{CH2}}$, and the $\overrightarrow{\text{DOT}}$ $\overrightarrow{\text{EN}}$ signals. The $\overrightarrow{\text{CH}}$ $\overrightarrow{\text{SW}}$ $\overrightarrow{\text{BLK}}$ signal for blanking the switching portion of the channel is generated from the $\overrightarrow{\text{CH1}}$ and the $\overrightarrow{\text{CH2}}$ signals. The 500 kHz clock pulse is constantly fed to terminal T of toggle flip-flop IC2160 in the RTO mode. The CKA pulse is fed out from COUTNTER/ TIMER IC5310 of $\overrightarrow{\text{13}}$ (Fig. 5-19) by the control of the MPU for the DSO. The state of the $\overrightarrow{\text{CH1}}$ and the $\overrightarrow{\text{CH2}}$ signals fed out from Q_{G} and Q_{F} of SHIFT REGISTER IC2165 are determined by the V.MODE and the

TIME/DIV switches.

Table 5-2 shows the relationship between "The Setting positions of the V MODE switch and the setting values of the TIME/DIV switch" and "The state of the $\overline{CH1}$, the $\overline{CH2}$, the $\overline{CH1}$ DSP, and the $\overline{CH2}$ DSP." Further, the supplemental explanation follows.

- (1) When the V. MODE switch is set to CH1, the CH1 signal is displayed. Since the $\overline{CH1}$ signal is low, and the $\overline{CH2}$ signal is high, IC2160 is in the reset state, and high and low are fed out from \overline{Q} and Q, respectively. (In this case, a clock pulse from T is not valid.) On the other hand, when characters are not displayed, the DOT EN signal fed to pins 10 and 13 of logic circuit IC2162 (3/4, 4/4) is high. Therefore, the $\overline{CH1}$ DSP signal is low, the $\overline{CH2}$ DSP is high, and the CH1 signal is displayed.
- (2) When the V. MODE switch is set to CH2, the CH2 signal is displayed. Since the CH1 signal is high, and the CH2 signal is low, IC 2160 is in the reset state.

- (3) When the V. MODE switch is set to CHOP, the CH1 and the CH2 signals are displayed alternately at a 250 kHz cycle. In this case, the $\overline{\text{CH1}}$ and the $\overline{\text{CH2}}$ signals are high, and IC2160 operates as a toggle flip-flop. Therefore, the outputs of $\overline{\text{Q}}$ and Q are inverted during the rising edge of a 500 kHz clock pulse fed to T.
- (4) When the V.MODE switch is set to DUAL,
 - a. When the TIME/DIV switch is set to 2 ms/DIV or slower, the circuit operation is the same as that of item (3).
 - b. When the TIME/DIV switch is set to 1 ms/DIV or faster, the polarities of the CH1 and the CH2 signals are opposite, and they are inverted every approx. 20 ms by the MPU for the RTO. Therefore, the CH1 or the CH2 signals are displayed alternately every approximately 20 ms.

For the channel selection in the DSO mode, refer to 5.13 (7).

V MODE	TIME/DIV	CH1	CH2	Q	Q	CH1 DSP	CH2 DSP	Displayed CH	
CH1		L	Н	Н	L	L L		CH1	
CH2		Н	L	L	Н	Н	L	CH2	
CHOP		Н	Н	H∢≯L	L≁≯H	∐≁≁H	ℍ⋖→⅃	CH1CH2 (250 kHz)	
DUAL	≧2 ms	Н	Н	H∢≯L	L≁→H	L∢≯H	H∢≁L	CH1CH2 (250 kHz)	
	≦1 ms	H≺≁L	L≁→H	H≁≁L	L∢≁H	L∢≯H	ℍ≼≁⅃	CH1CH2 (20 ms)	

Table 5-2

5.9 MPU(RTO), CHR GEN & FRONT PANEL ($\langle 8 \rangle$, $\langle 9 \rangle$ 5/5)

Outline

The description on the MPU for the RTO, its peripheral circuits, the control circuit of information on characters and cursors, and the circuit which inputs information on the panel switch setting into the MPU for the RTO follows. Refer to schematic diagrams $\langle 8 \rangle$ and $\langle 9 \rangle$, detailed block diagram Fig. 5-15, block diagrams Figs. 5-9, 5-12 and 5-13, waveform charts Figs. 5-10 and 5-11 and simplified schematic diagram Fig. 5-14.

Most of information on the switches at the right half side of the panel is acquired, in the RTO mode, by the MPU for the RTO, which controls the waveform display and the readout to obtain the optimum state. The switches of the storage mode under the screen, left half side of the front panel, are controlled by the MPU for the DSO.

Information on the panel switch setting is acquired as an analog signal from ports ANO to AN7. The analog signal is converted into a digital signal by the A/D converter built in the MPU for the RTO. The processing programs are stored in ROM IC3006. The 10 bits digital data among the control signals fed out from the MPU for the RTO is converted into analog data by RM2120. The converted analog data is output from ANALOG DA1 SWITCH IC2130 as a continuously variable signal.

A digital control signal is fed out from port PCO as an S-DATA (serial data), sent to the four shift registers* in Fig. 5-12, and fed out as bit information.

* IC2165 of $\langle 6 \rangle$, IC2166 of $\langle 8 \rangle$, and IC1601 and IC1602 of $\langle 9 \rangle$

The frequency of the measured signal (max. 100 MHz) is measured by measuring the frequency of the trigger signal developed from the measured signal.

The counter built in the MPU for the RTO counts up to 1 MHz. Therefore, the trigger signal is counted down to 4:1 by the counter of $\langle 5 \rangle$ (Fig. 5-4). The resultant signal is further counted down to 32:1 by the COUNTER 1 of $\langle 8 \rangle$ (Fig. 5-15). Thus the trigger signal is counted down to 128:1 by the external counters. The resultant signal is fed to PC5, entrance to the counter of the MPU.

The MPU reads the frequency of the measured signal by counting the counted-down signal, and determines the sweep time automatically.

While the change of the setting state is being fed out from the MPU, the waveform display is blanked so as not to appear the disturbance of the waveform. For this purpose, the control signal is sent to the Z-CONT circuit from the output port PC3 via 80 . The H signal is fed out from PC3 in case of blanking. The character display data is fed out from LATCH 2 IC3005 and LATCH 3 IC3004, converted into analog data by RM2232 ($\langle 9 \rangle$) and RM2231 ($\langle 9 \rangle$), and then fed out as analog voltages CHR-X and CHR-Y from ANALOG SWITCH IC2220 ($\langle 9 \rangle$). The A/B ALT SEP BIAS voltage is fed out from the same terminal as that of CHR-Y. The switching of characters, vertical and horizontal cursor patterns, and A/B ALT SEP BIAS outputs is performed by ANALOG SWITCH IC2220 (<9>).

The machine clock of this MPU is 12 MHz, and oscillated by ceramic oscillator X3101. While the power is on, terminal RESET is maintained to be low by the RESET circuit until the voltage for the digital circuit power supply becomes stable.

Read of status information

Information concerning the setting state of switches on the panel is fed to ports ANO to AN7 of the MPU as an analoq signal. When one of the variable control items such as DELAY, HOLDOFF, TIME, H POS related to the X axis and the cursors (ΔV , ΔT and $1/\Delta T$) is selected by the SELECTOR switch, the MPU recognizes the DC output voltage of the endless variable resistor (VARIABLES) as the signal that controls the selected item, and processes the output voltage. When SINGL or SEP is selected by the SELECTOR switch, the VARIABLES is not valid. The MPU converts an analog signal into a digital signal by the built-in A/D converter, and performs various processes using the signal. AV_{DD} and VA_{REE} are input terminals of the Terminals supply voltage and the reference voltage of the A/D converter, respectively.

Read of programs and transmission of data

As many pins of MPU IC3101 are allotted to inputs and outputs, the number of pins for bus is limited. Therefore, the same bus is used on the time division basis. LATCH 1 IC3003 is the circuit which functions to separate only the address information among the common bus. The liest significant 8 bits of the memory address are output form PD7-PD0, and the most significant 8 bits are output from PF7-PF0.

The parallel data output from PD7-PD0 and PF7-PF0 are retained in IC3005 and IC3004, respectively.

The decoder to which RD, WR, and ALE signals are input determines the IC to be selected from ROM, RAM and latch circuits. Fig. 5-9 illustrates the above description.

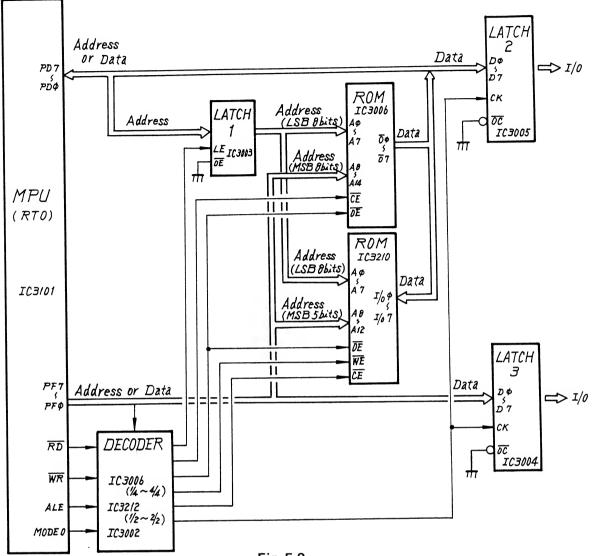


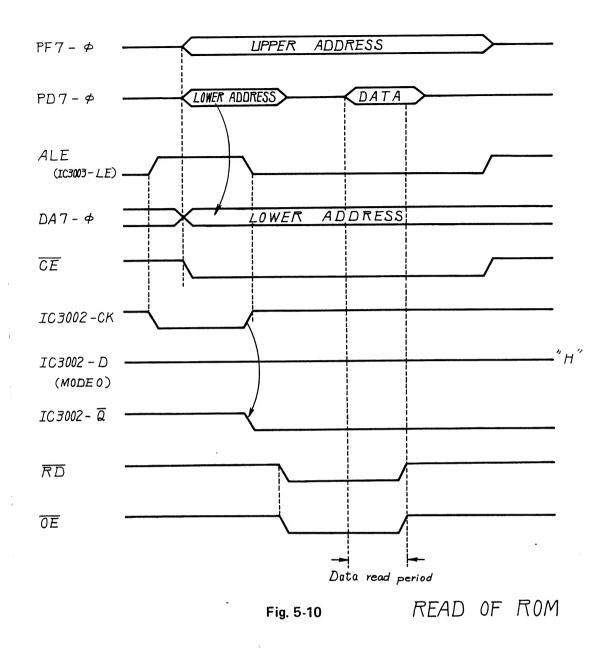
Fig. 5-9

information is sent to LATCH IC3003 from ports PD7 to Address At this time, terminal LE of IC3003 is high of the MPU. PD0 (latch enable), so that IC3003 latches this address information. Since terminal $\overline{\text{OE}}$ of IC3003 is always low, information on the latched address is transferred to ROM IC3006 immediately. bits of address information is ROM sent to high-order The from ports PF6 to PF0 of the MPU. CE At this time, IC3006 (chip enable terminal) is low by the signals at PF7 and PF6.

(1) READ of ROM (Figs. 5-10 and 5-15)

The ALE of the MPU is the signal which determines the timing that the bus is used for address or data. Assume that the ALE goes high, the LE of LATCH 1 IC3003 goes high accordingly, and LATCH 1 is in the latch enable state. In this case, if the high-order address and the low-order address are output to PF7-0 and PD7-0, respectively, the \overline{OE} (output enable) of LATCH 1 remains low. Therefore, the low-order address information of PD7-0 is output to DA7-0. Further, when PF6 low and PF7 low passes through IC3004 (4/4), the \overline{CE} of ROM IC3006 goes low, and the ROM is in the chip enable state.

The polarity of the ALE is inverted by IC3212 (2/2), and the resultant signal is fed to the CK of IC3002. IC3002 latches the state of the MODE O supplied to D by the rising edge of CK (ie. rising edge of the ALE). The MODE O goes high when the ROM is in the READ mode, and low is output from Q of IC3002. When the RD goes low in this state, the OE of the ROM goes low by the operation of IC3006 (2/4). As a result, the MPU reads the data (program) of the ROM through bus PD7-0. When processing is executed in accordance with the program read by the MPU, the data on the results of processing is fed out from each port.



(2) READ of RAM

When PF6 high and PF7 high passes through RAM IC3210, the output of IC3212 goes low, and the \overline{CE} of IC3210 goes low. The WR goes low when the RAM is in the READ mode. The description of (1) READ of ROM is applied except for the above.

(3) WRITE of RAM

The process until the low-order address information of PD7-0 is output to DA7-0 and the OE goes low is the same as described in (1). The process until the \overline{CE} goes low is the same as described in (2).

When the WR goes low with the Q of IC3002 low, the WE of RAM IC3210 goes low by the operation of IC3006 (1/4).

As a result, the MPU writes the data on the RAM through bus PD7-0.

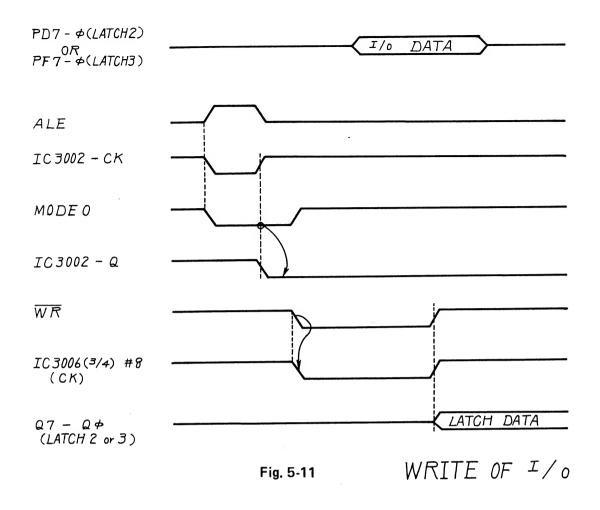
While the RAM is in the WRITE mode, the RD of the MPU remains in the high state.

(4) WRITE of I/O (Figs. 5-11 and 5-15)

In this mode, the MODE O goes low from high at the timing that the ALE goes high. The MODE O remains in the high state even if the ALE goes back low.

Consequently, low is output from Q by the rising edge of the CK of IC3002. During this period, the data for LATCH 2 and for LATCH 3 are output from PD7-0 and PF7-0, respectively. As low is being output from Q of IC3002, the output of IC3006 (3/4) #8 goes high when the WR goes high. As the output of IC3006 (3/4) #8 is in the CK of LATCH, the CK goes high accordingly. The I/O data of PD7-0 and PF7-0 are latched by LATCH 2 and LATCH 3, respectively, by the rising edge from low to high.

In this case, the OE signals of ROM IC3006 and RAM IC3210 go high, and 07-0 and I/O 7-I/O0 become the high impedance state. Therefore, the ROM and RAM have no relation with the I/O data transfer.



Output of the analog control signal

The 8 bits output of PA7 to PA0 of the MPU for the RTO and the 2 bits output of Q7 and Q6 of IC3005 are added. The resultant 10 bits data is converted into the analog voltage by D/A 1 (RM2120), and fed to ANALOG SWITCH IC2130. D/A 1 has a resolving power of 1000, and feeds out the analog voltage between 0 and 5 V. ANALOG SWITCH IC2220 is constantly switched in the fixed order by a 3 bits control signal from PB2 to PB0. The output voltage of the ANALOG SWITCH is maintained the at fixed voltage by a sample hold capacitor of each line. The INH signal in the high state is fed out from PB4 when the switch is changed to perform a "break before make" operation.

Transmission of serial data

The S DATA (serial data) is the digital control signal that is fed out from port PCO of IC3101 of the MPU for the RTO. This signal is converted into the parallel signal by SHIFT $IC2165(\langle 6 \rangle), IC2166(\langle 8 \rangle), IC1601(\langle 9 \rangle)$ REGISTER's and IC1602($\langle 9 \rangle$) as the digital control signal. There are three kinds of S DATA: A , B and C . A is the 16-bit parallel signal fed out from IC1602 and IC1601 which consist of the 9-bit signal to light the LED on the front panel and the SI SELA (1 bit) which is one of the control signals to switch an input signal to input import PC5 of the MPU. All of the 16 bits are not always used. B is the 8-bit parallel signal related to the switching of the TIME/DIV setting value of the waveform sweep and of the DISPLAY mode. This signal is fed from IC2165.

Shift registers IC2165, IC1601 and IC1602 are connected in series, and the 24 bits S DATA (A data + B data) is acquired from data input terminal SER of IC2165.

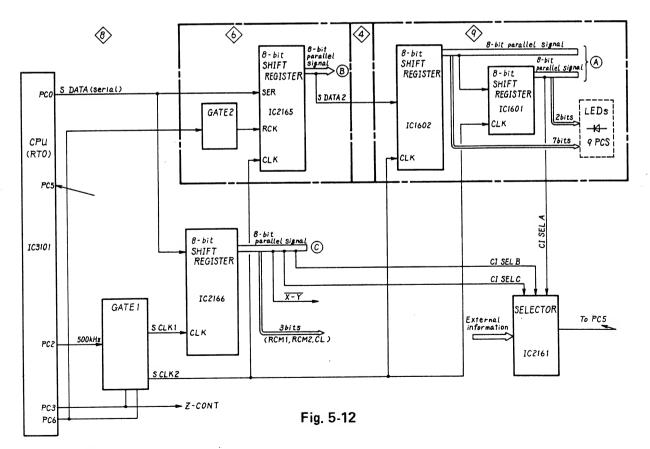
Then (A) data is allocated to IC1602 and (B) data to IC1602 and (B) data to IC2165. Data of each shift register is acquired by the clock pulse SCLK 2. To change the content of a digital control signal, a 24-bit S DATA is sent only once whatever the bit to be chanted is.

The SCLK 2 is the pulse obtained when the 500 kHz pulse that is fed out constantly from PC2 passes GATE1 (IC2107) of $\langle 8 \rangle$. This pulse is controlled by the output signal from PC6 and fed out only when the signal on PC6 goes high. PC6 is also used as a latch enable signal fed to the RCK terminal of IC2165 ($\langle 6 \rangle$). Refer to $\langle 6 \rangle$ for the latch operation.

(C) data is the 8-bit parallel signal which consists of the information for determining the cycle period and of X-Y mode and the control signal (Ci SEL B, Ci SEL C) for the switching of IC2161((8)). (C) data is fed to IC2166((8)), and shifted by

shift clock pulse SCLK1. This data is updated only when the bit of the digital control signal is needed to change, and any When all 8-bit data is shifted, an 8-bit S DATA is sent once. 500 The SCLK1 signal is also a kHz signal stops. SCLK1 the In this case, GATE 1 is controlled pulse which passes GATE 1. the PC3 output and the timing is determined by the output. bv Therefore, when updating IC2165 latches the 8 bits at a time. (B) data, the 8-bit shift data is latched at a time when new 8serial signal is completely shifted in sequence and when bit the waveform display is within the blanking period. Therefore, switching of (B) data does not effect the display on the the CRT.

On the other hand, the switching of C data is performed by the shift of an 8-bit S DATA. Therefore, when the switching is performed during the sweep period, the normal display is not obtained. When the PC3 output is high, the PC3 signal (SCLK1) is sent to the Z circuit to blank the display.



Acquisition of a control signal

The MPU acquires external information from PC5 via SELECTOR When the power switch is turned to on, the $IC2161(\langle 8 \rangle).$ MPU reads the DC voltage of terminals D7 to D5 of IC2161, discriminates the type of this oscilloscope, and selects the applicable program memorized in the ROM. Then, the MPU reads the DLY ADJUST and SWP GATE signals from D3 and D4, and executes the automatic calibration of the delay time and the sweep time. The automatic delay time calibration is executed by converging the DLY RAMP signal by the TEST SIG fed from PC4 via 22, the analog output DLY PRESET, from 38 and the loop circuit consisting of the feedback signals DLY ADJ and SWP GATE.

Normally the switching control signals Ci SEL B and Ci SEL C of IC2161 are low. When the Ci SEL A goes low or high, D_0 or D_1 of the analog switch is connected, and the trigger pulse of the measured pulse is counted to determine the cycle time. Moreover, the H/0 END signal from 39, 85 and 86 and the LATCH CHECK signal from 47 are fed to the MPU to transmit the external status.

Transmission of information on characters and cursor patterns

Data of character information is output from LATCH 3 IC3004 and LATCH 2 IC3005. In other words, 3 bits data related to the Y component of information representing a character is output on PF2' to PF0', 3 bits data related to the X component of information representing a character is output on PF6' to PF4', and 5 bits data related to the X position of each character (number from first among 32 characters per line) is output on PD4' to PD0'.

After digital data related to the Y component of a character is converted to analog data by the D/A converter D/A 1 RM2232 (9), the DC voltage CUR-POS representing information about the vertical position (upper line or lower line) of a character or a cursor position is added to an analog data, and input to analog switch IC2220(9). The CUR-POS is fed out from ANALOG SW1 IC2130(8). Three bits data related to the X component of a character and 5 bits data related to the X position of each character are added, and the resultant 8 bits data is converted to the analog signal by D/A 2 RM2231(9).

Dots for cursors generated by the CURSOR DOT GENERATOR ($\langle 9 \rangle$) are converted by D/A 3 RM2211($\langle 9 \rangle$), and fed to IC2220($\langle 9 \rangle$). Moreover, the 1 V DC voltage determining the center position of horizontal axis of the A sweep waveform is applied to the the The A/B ALT SEP BIAS of IC2220. voltage X2 terminal determining the center position of the horizontal axis of the B sweep waveform in the A/B ALT mode is applied to the terminal switching of IC2220 corresponding to these X3. The input signals is performed by the control signal A via SECTION LOGIC the CUR SEL signal, and the DOT EN signal. Table 5 - 3(< 9 >), The horizontal or vertical position detail. of shows the cursors on the CRT is determined by IC2220. The vertical or movement of cursors is determined by the CUR-POS horizontal signal.

Next, the description on the cursor pattern generator circuit follows. When the MEASURE switch on the front panel is selected, the CUR RESET signal fed from the MPU goes low, the pin 10 of CURSOR DOT GENERATOR IC2248 goes high, and the The oscillated clock pulse is fed to CLK oscillation starts. COUNTER IC2212. The output from COUNTER is converted of into an analog signal by D/A 3 RM2211($\langle 9 \rangle$). The converted analog signal is fed out as a cursor pattern signal. Since the pin 4 of D/A 3 is grounded, cursor patterns are dotted lines.

When output D6 of counter IC2212 ($\langle 9 \rangle$) goes high, pin 10 of CURSOR DOT GENERATOR IC2248 ($\langle 9 \rangle$) goes low, and the oscillation stops. At the same time, the COUNTER sends the CUR END signal in the high state to the MPU from 92.

The MPU receives the CUR END signal and sends the CUR RESET signal in the high state to reset counter IC2212 via 96. When the COUNTER is reset, D6 goes low, but pin 5 of IC2211 (2/4) is high. Consequently pin 10 of IC2248 (3/3) is low, and the CURSOR DOT GENERATOR continues to stop the oscillation. When the CUR RESET goes low and the reset is released, the oscillation starts and the above operation is repeated.

Kinds of DISPLAY		Control signal			Control signal of switch IC2220		Connec- tion of	Output signal	Output signal
		DOT EN	CUR SEL	Ā	Ter- minal B	Ter- minal A	switch IC2220	of X termi- nal	of Y termi- nal
Wave- form display	A sweep	Н	*	L	Н	L	$\begin{array}{c} \mathbf{X}_2 - \mathbf{X} \\ \mathbf{Y}_2^2 - \mathbf{Y} \end{array}$	1 V DC	No
	A/B ALT	Н	*	H	Н	Η	$\begin{array}{c} X_3 - X \\ X_3 - Y \end{array}$	A/B ALT SEP BIAS	No
Character display		L	L	*	L	L	Х ₀ — Х Y ₀ — Y	Y compo- nent of a chara- cter (added to the CUR POS)	X compo- nent of a chara- cter
Horizontal cursor display		L	L	*	L	L	$\begin{array}{c} x_0 - x \\ y_0 - y \end{array}$	CUR POS	Cursor pattern
Vertical cursor display		L	Н	*	L	Н	$\begin{array}{c} x_1 & \dots & x \\ x_1 & \dots & y \end{array}$	Cursor pattern	CUR POS

Table 5-3

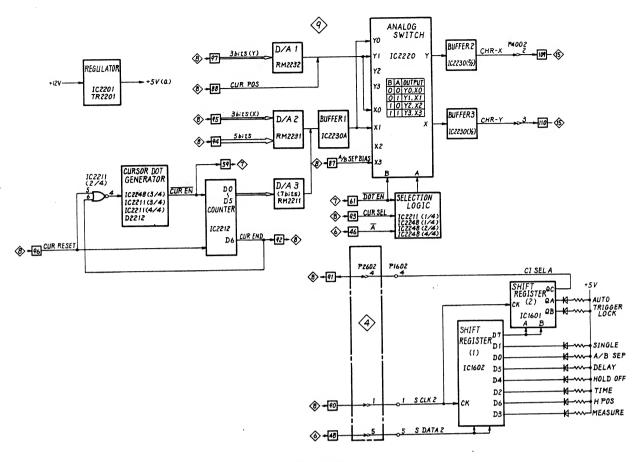


Fig. 5-13

Others

- (1) The information on the settings of almost all the switches at the right half of the front panel is sent to the MPU for The MPU judges the V MODE status by the voltage RTO. the the AN1 signal as shown in Fig. 5-14. In а similar of H MODE, CH1 UNCAL, TRIGGER LOCK, etc. are judged fashion, by the AN2 signal, and CH2 UNCAL, X10 MAG, .5S, 50 ns, etc. are judged by the ANO signal.
- (2) The RXD and TXD signals are used, in the DSO mode, for the data transfer between the MPU for the RTO and the MPU for the DSO.

(3) POWER UP RESET CIRCUIT

POWER UP RESET CIRCUIT's (1) and (2) hold the $\overline{\text{RESET}}$ terminal of the MPU (RTO) to be low until +12 V and +5 V (d) reach the normal voltages after power up.

(4) MEMORY BACK UP

Under the normal operation, +5 V (d) is applied to V_{CC} of RAM IC3210 via D3062. At this time, back-up capaciter C3050 is charged. When +5 V (d) becomes lower than a specified value, +5 V is applied to V_{CC} from C3050. (Back-up duration is 48 hours.) At the same time, TR3201 becomes off and the CE signal of RAM goes high. As a result, RAM IC3210 is electrically separated, and the holding current becomes minumum.

The backup voltage +5 V BU supplied from C3050 is also routed to 14 via 101 to backup RAM IC5503 of the MPU for the DSO.

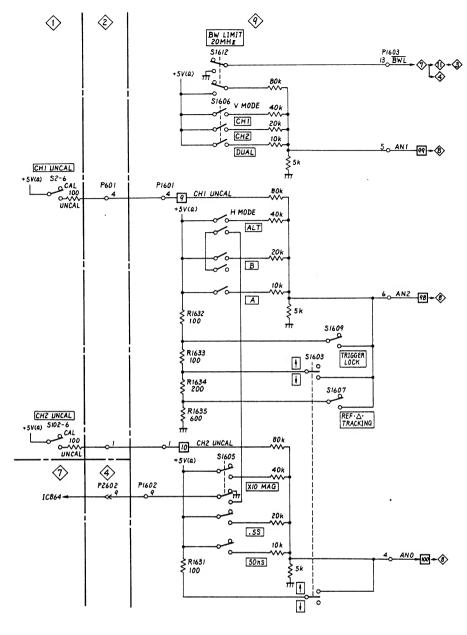


Fig. 5-14

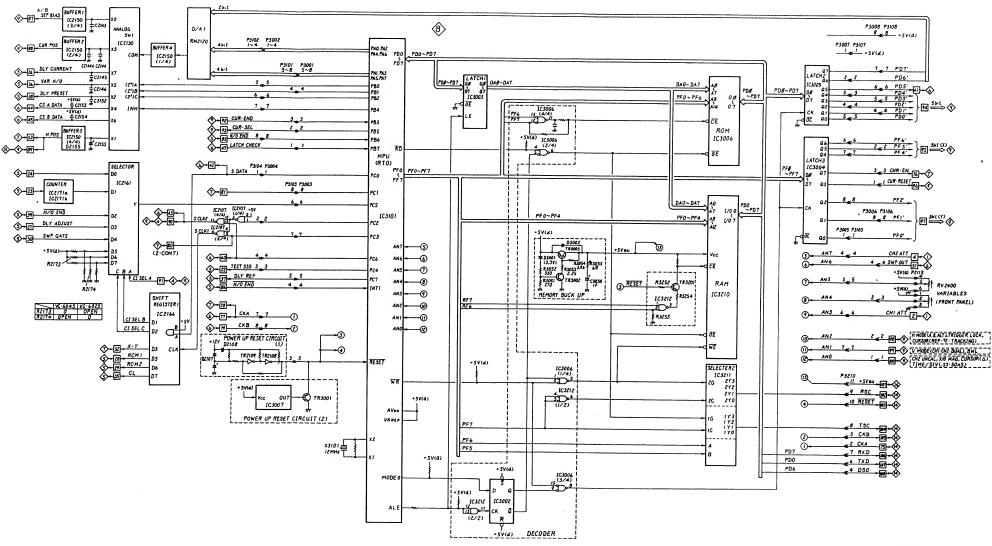


Fig. 5-15

5.10 HV, CRT ((0) 2/2)

The detailed block diagram of this circuit is shown in Fig. 5-16. This circuit consists of the following five blocks.

- (1) High voltage generation circuit and the voltage regulator circuit (VCO, PULSE AMP, SWITCH, FLYBACK TRANSFORMER & RECTIFIER, ERROR DETECTOR)
- (2) Bias circuit for Grid No.1
 (CHOPPER 1, DC RESTORER)
- (3) Focus control circuit (VOLTAGE DIVIDER, CHOPPER 2, DC RESTORER 2, focus and intensity control circuit)
- (4) CRT
- (5) Others

(TRACE ROTATION, ASTIG)

The circuit operations of the above blocks (1), (2), and (3) are described below. For details, refer to the schematic diagram HV, Z, CRT 10.

- (1) High voltage generation circuit and the voltage regulator circuit
 - (a) Voltage controlled oscillator (VCO)

The VCO supplies a positive pulse voltage from the collector of TR1002 by turning on and off TR1001 and TR1002 alternately. When the power switch is turned on, TR1001 becomes on, and C1004 starts to be charged through R1004. The charging voltage of C1004 rises the emitter voltage of TR1002 and then TR1002 becomes on. C1004 discharges immediately after TR1002 becomes on, the emitter voltage of TR1001 drops, and TR1001 becomes off. Then, C1004 is charged in the opposite direction through R1003, the emitter voltage of TR1001

rises, and TR1001 becomes on. These operations are repeated to continue generating the positive pulse. period of the pulse is determined by the on/off The TR1001 and TR1002. In other words, periods of the period is determined by the time constants of R1003 and R1004 and C1004 and C1004, the charging and current. If the charging current is small, the pulse. frequency becomes low, and the pulse width of the positive portion of the output pulse increases. Then, the energy in the primary coil of the FLYBACK TRANS-(FBT) increases and the output voltage of the FORMER secondary coil increases.

(b) PULSE AMP

The positive pulse is amplified by PULSE AMP TR1010. and is supplied to the base of switching transistor TR1013 through pulse transformer T1013. The PULSE AMP the VCO output up to the level enough amplifies to drive the switching transistor and shapes the drive current waveform to minimize the cut-off loss of the switching transistor. The PULSE AMP also functions as buffer to prevent the load variation at the output а stage of the switching transistor from affecting the vco.

(c) SWITCH

When the positive pulse is supplied to the base of switching transistor TR1013, TR1013 becomes on, the current which increases linearly flows into the primary coil of the FBT, and the energy is stored. Even if the switching transistor becomes off, the current continues to flow in the same direction by the inductance inertia of the coil, and C1013 is charged. The charging current decreases gradually, and the charging voltage becomes maximum when the charging Then, a discharging current current becomes zero. flows in the opposite direction through the coil. When the voltage on C1013 becomes zero, the discharging current becomes maximum. D1013 becomes conductive by the counter electromotive force of the coil, and the current flows from the coil in the charging direction. The current decreases gradually, and becomes zero again. Later, TR1013 becomes on by the next positive pulse, and the same circuit operation is repeated. Thus, the alternate current flows into the coil and the voltage is generated at the secondary circuit.

(d) Voltage regulator circuit

This circuit detects a change in the cathode voltage of the CRT, and feeds back the change to the VCO to control the oscillation frequency so that the output voltage is regulated.

A small current flows from the base of TR1023 to the cathode line (-1650 V line in the schematic diagram) through R1035. The current is the sum of the base current of TR1023, the current through R1024, and the base current of TR1022.

For example, when the cathode voltage changes in the positive direction, the current flowing across R1035 decreases. Since the base current of TR1023 and the current across R1024 are constant, the base current of TR1022 decreases. Then, the emitter current of TR1022 decreases, and the charging current of C1004 in the VCO also decreases. Consequently, the oscillation frequency of the VCO becomes low as described in (a),

and the cathode voltage of the CRT changes in the negative direction. The secondary output voltage of the FBT is thus regulated by the feed-back loop.

(e) FBT

A half-wave rectified output of 15 kV is supplied from the secondary side of the FBT, and is applied to electrode P3 of the CRT. A half-wave rectified the signal of -1650 V is supplied to the cathode. The heater voltage is connected to the cathode line and is the same electric potential with the cathode obtained -350 V pulse voltage is to А voltage. focus G1 bias voltage and the bias produce the voltage.

(2) Bias circuit for Grid No.1

(CHOPPER 1, DC RESTORER 1)

This circuit generates a voltage applied to G1 of the CRT. A pulse voltage is supplied from T1013 via C1040 and R1040. The positive peak voltage is limited to the CRT bias voltage (E_A) by D1040 and the negative peak voltage is limited to the output voltage (E_Z) of the Z-AXIS AMP. Then, the chopped waveform having the envelope of the difference between E_A and E_Z appears at point P (See the block diagram).

chopped waveform is supplied to D1043 via C1041, and The positive peak voltage is clamped to the -1650 V the cathode voltage. The negative peak voltage is rectified by D1042 and D1043 to produce a negative DC voltage. As a signal whose DC level is shifted to the result, the voltage lower than the cathode voltage is supplied to G1. (The waveform of the signal is the same as that of the Z – AMP output.) The high-frequency component of E7. is AXIS directly supplied to G1 via C1043.

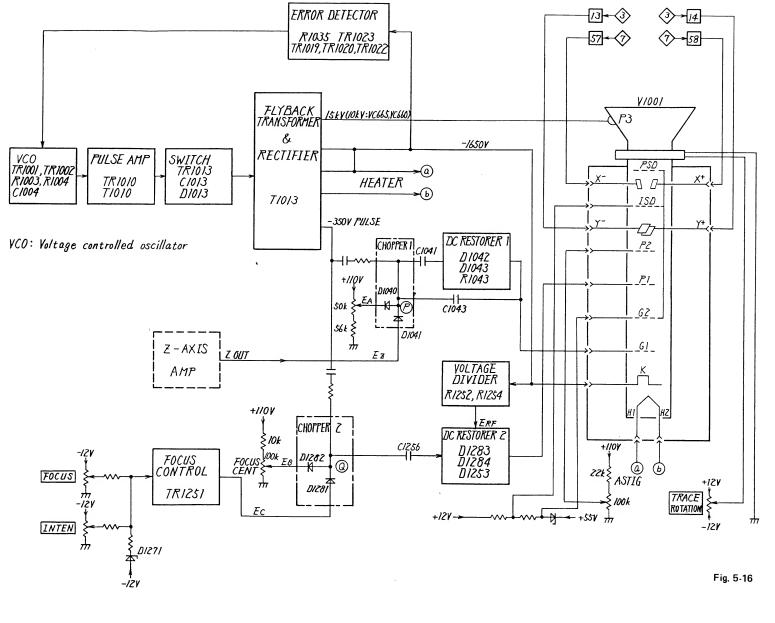
(3) Focus control circuit

This circuit produces a voltage applied to P1 (focus) of The focus voltage is produced with the reference the CRT. to E_{FR} (-1165 V) obtained by dividing the cathode voltage (-1650 V) and E_B at the FOCUS CENT control. Since an optimum focus voltage changes due to the variations in characteristics of the CRT, set E_R so that the optimum focus is obtained when the FOCUS and INTEN controls are set to their respective mid-positions. A pulse is supplied from T1013 via C1255 and R1260. The positive peak voltage is limited to E_B by D1282 and the negative peak limited to E_C set by the voltage is INTEN and FOCUS controls.

Then, a chopped waveform having the envelope of the difference between E_B and E_C appears at point \bigcirc (see the block diagram).

The chopped waveform is supplied to D1284 via C1256, and the negative peak voltage is clamped to $E_{\rm FR}$ (-1165 V). The positive peak voltage is rectified by D1283 to generate a positive DC voltage. As a result, the voltage whose DC level is shifted to the level higher than $E_{\rm FR}$ is produced, and is applied to the P1 electrode as the focus voltage.

The relationship between the intensity of the CRT and the voltage for the optimum focus is not linear. Consequently, the change in E_C caused when the INTEN control is adjusted is approximated to the actual CRT characteristics using the polygonal line characteristics.



5.11 POWER ((1))

Outline

This circuit supplies the voltages to the circuit performing the NON STORE operation.

This circuit is a power supply circuit using a switching regulator, and uses hybrid IC IC1501 (STK7308) as a switching circuit. Figure 5-17 is the simplified circuit diagram of this circuit.

When switching transistor TR5 in IC1501 is on, the energy is stored in pulse transformer T1501 by the collector current. The stored energy is emitted to the secondary circuit while TR5 is off. The feedback loop circuit controls the duration of the on and off periods to control the transfer amount of energy, ie, to stabilize the output.

The description of the major functions follows.

- (1) Switching operation
- (2) Stabilizing operation of output
- (3) Protection circuit of switching transistor

(1) Switching operation

The on and off operation is described.

- (i) When the power switch is turned to on, the positive voltage is applied to the base of switching transistor TR5 in IC1501 via starting resistors R1503 and R1504, and TR5 is turned to on. Thus, the collector current Ic flows to the primary winding N1 of T1501.
- (ii) The voltage induced between terminals 2 (positive) and3 (negative) turns TR4 to on, increases the base current of TR5, and increases the collector current Ic.

- (iii) When the collector current IC of TR5 reaches to saturation, the induced voltage of N2 turns to zero, and TR5 turns to off.
- (iv) The energy stored in T1501 becomes a current and fed to the secondary wiring N4 (N5 through N8), and is emitted through D1513.
- (v) The voltage induced at N2 (terminal 2 : positive) turns TR5 on again.

The above operations are repeated.

The collector current of TR4, ie, the base current of TR5, becomes the constant-current controlled zener diode by D1514 and resistor R9 in IC1501. (ZD3 is off because the zener voltage of zener diode D1514 is 2.4 V, and that of zener diode ZD3 in IC1501 is 5.1 V.) When the positive feedback induced at N2 exceeds the fixed value, D1515 is conducted and then TR1514 is turned to on. Thus, the base current of TR4 is decreased, the collector TR4, ie, the base current of TR5 is also current of decreased, and the collector current of TR5 is decreased. These operations prevent the collector current of TR5 from flowing excessively.

(2) Stabilizing operation of output

The DC voltage (approx. -28V) is produced by rectifying the AC voltage fed back from winding N4 to windings N2 and N3 when TR5 is off. This DC voltage is divided, and added to the base of ERROR DETECTOR TR1 to stabilize the voltage of regulator output. In other words, the emitter potential of TR1 maintained constant by zener diode ZD1 is compared with the base potential of TR1 and the error signal is detected. This error signal is amplified by TR2, and supplied to the base of TR3, and the collector current of TR3 is thus controlled.

When the output voltage of the regulator rises, the collector current of TR3 increases, and the base current of TR4 is decreased.

Consequently, the base current of TR5 is also decreased and the saturation point of the collector current of TR5 is decreased. In other words, the amount of energy transferred to the secondary circuits of T1501 is reduced by the on-duration of TR5 short. making The voltage across R1502 is supplied to the base of TR2 through R1507 to match the timing to turn TR5 to off, ie, the timing to control the collector current of TR3 with the timing of the peak of the collector current of TR5.

(3) Protection circuit of the switching transistor

Circuit protection after turning power to on

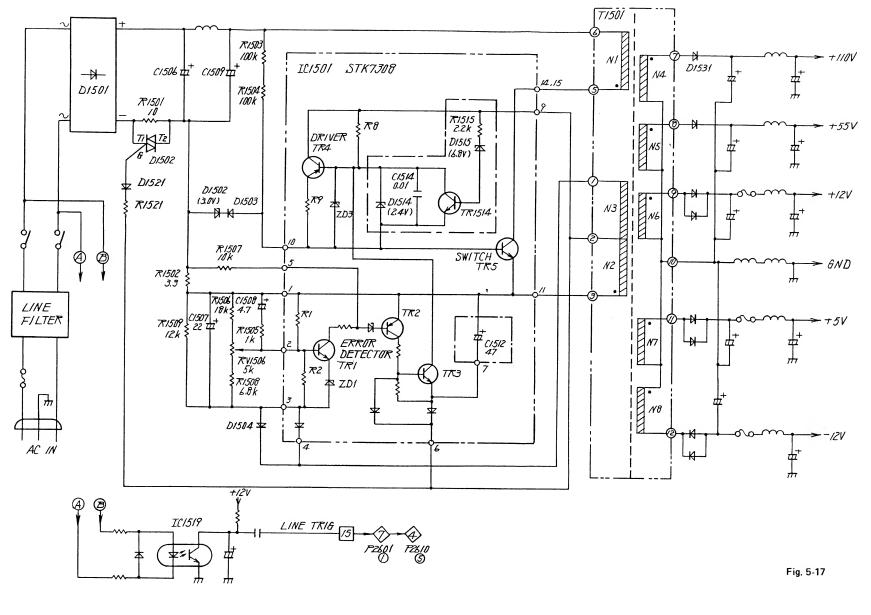
- (i) Immediately after the power switch is turned to on, triac thyristor D1502 is off, and the charging current of C1508 (and C1509) flows to R1501. This prevents the rush current from doing damage to the circuits. voltage induced at N2 is supplied to The D1502 as а negative trigger pulse. Then, D1502 turns to on, and this power circuit becomes a steady state.
- (ii) Immediately after the power switch is turned to on, the base voltage of TR1 is much higher than the emitter voltage of TR1, compared with the steady operation state, because the charging speed of C1508 and C1507 is different. a result, the collector current of TR3 increases, As and base current of TR4 decreases. the The base current of TR5 decreases, and the collector current of TR5 is limited to a small amount. After C1508 and C1507 are charged, this power circuit becomes a steady state.

Circuit for protecting the excessive current

D1502 is a 3.0 V zener diode, and determines the upper limit of the base current of TR5 together with D1503 and R1502. This prevents the excessive current from flowing to TR5.

Others

The LINE TRIG signal for the line lock is taken out from the primary line. After the signal passes through photo coupler IC1519, the waveform is shaped and supplied to the TRIG circuit via 15.



5.12 TRACK HOLDER ($\sqrt{2}$)

Fig. 5-18 is a detailed block diagram of this circuit. Refer to the attached schematic diagram $\sqrt{2}$, too.

The AC signal (either of the CH1 V. SIG or CH2 V SIG signal) fed from $\langle 2 \rangle$ is routed to relay D8060a via $\boxed{64}$ and $\boxed{65}$. The relay is controlled by the DSO signal fed from $\boxed{113}$. In the RTO mode, the AC signal passes through the relay, and fed out to $\langle 3 \rangle$ via $\boxed{67}$ and $\boxed{68}$.

In the DSO mode, the AC1 signal is applied to the STR V AMP, and the paraphase signal is converted into the single-ended signal. TR8062 is an emitter follower.

The output of the STR V AMP is applied to the SAMPLE HOLDER SW the next stage. This is a high speed switch which in can correspond to the sampling rate. The operation of this switch is controlled by the SW DRIVER. When (A) is high and (B) is low (Fig. 5-18), the switch is in the close state, and the signal passes through the switch. When (A) is low and (B)is high, the switch is in the open state, and the signal does not pass.

The signal which passes through the SAMPLE HOLDER SW is applied The BUFFER is of a high input impedance and to the BUFFER. а low output impedance, and the gain is designed 1 to be correctly. (The output is 1 with respect to the 1 input.) TR8063 is a source follower and TR8066 is an emitter follower. S/H ADJ RV8060 controls an entire offset. Α fine offset control for each mode is made in $\langle 1 \rangle$. The amplitude of the input of the A/D converter is limited (The maximum amplitude is determined), and the output of the BUFFER is designed to be 0 ± 0.5 V. Namely, the voltage of -0.5 to +0.5 V at the output point of the BUFFER corresponds to 10 div on the CRT. (Correct A/D conversion is not ensured to the signal in excess of the

voltage range.) The SH CLK signal from 12 is converted into the differential signals (SH CLK and SH CLK) by the CURRENT SW. The rising edge of the SH CLK is a sampling point.

REALTIME SAMPLING

In the real time sampling mode, the SH1 CLK is always low and SH CLK is high. Consequently, TR8068 is off and TR8069 is on. (A) goes high and (B) goes low. Thus, the SAMPLE HOLDER SW is in the close state, and the signal always passes.

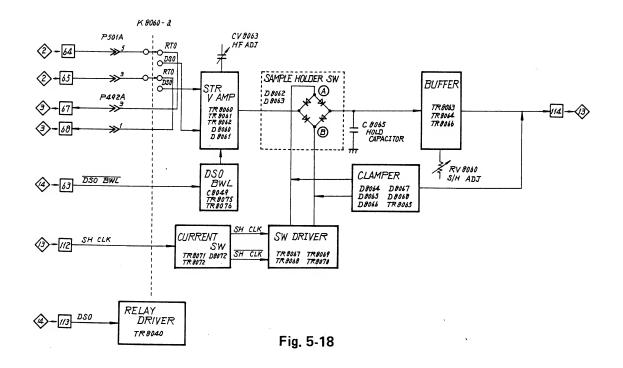
In the equivalent time sampling mode, the SH1 CLK goes high and the SH CLK goes low at the sampling point. Consequently, TR8068 is on and TR8069 is off. A in Fig. 5-18 goes low and B goes high. Thus the SAMPLE HOLDER SW is in the open state, and HOLD CAPACITOR C8064 holds the voltage at the sampling point.

Before the SH CLK goes low and the SH CLK goes high at the end of a sweep, the voltage of the HOLD CAPACITOR is converted into the digital signal in the A/D converter ((13)) via the BUFFER and the AMP ((13)), because the operation speeds of the BUFFER, the 2X AMP and the A/D converter are slower than the switching speed of the SAMPLE HOLDER SW.

The CLAMPER (1) is provided to:

- (1) limit the voltages at (A) and (B) in a given range when the SAMPLE HOLDER SW is off, and
- (2) limit the output range of the BUFFER (1).

TR8065 is an emitter follower, and the clamp voltage tracks the output voltage. The tracking range is limited to ± 0.7 by D8067.



5.13 AD DRIVER & ACQ MEMORY ((13))

For this circuit, refer to the schematic diagram (13), the detailed block diagram Fig. 5-19 and the timing chart Fig. 5-20.

STR V.AMP

The STR V AMP (1) consists of TR5201, TR5202, TR5203, etc. The S/H (sample holder) output of around zero volts is fed to the input (TR5201 base) of this amp via $\boxed{114}$. From this amp, the signal around +2.5 V (+2.5 V ±1 V) which is suitable to the A/D input in the following stage is fed out.

The gain of this amp is approximately 3 times, and controlled by AD1 GAIN RV5201. The CURRENT SOURCE (1) consisting of TR5202 and its peripheral circuits functions to offset the center of the output voltage of this amp to +2.5 V.

To make the center voltages in the normal sampling mode and the equivalent sampling mode equal, the offset voltages in both

are controlled by AD1 NORM OFFSET RV5202 and AD1 ΕO modes These two controls are switched by the ANALOG OFFSET RV5203. SW(1) that is controlled by the EQ CK EN signal. As the A/D (2) is not used in the equivalent sampling mode, the switch of this kind is not provided for the STR V AMP (2). upper and lower limits of the output voltage of this amp The are controlled by TR5206 and TR5207, respectively. Normally, voltage between the base and emitter of each limiter is the biased reversely, and both transistors are in the off state.

A/D CONVERTER

The input range of the A/D (1) is from +1.5 to +3.5 V. Consequently, the lower limit voltage is applied to the $V_{\textrm{RT}}$ terminal from the VOLTAGE FOLLOWER (1), and the upper limit voltage is applied to the $V_{\sf RB}$ terminal from the VOLTAGE FOLLOWER (2). The A/D (1) is an 8-bit flash A/D converter, and the A/D conversion is performed at each rising edge of the clock signal.

ACO MEMORY

The ACQ MEM (1) is a 2KB (2048 words x 8 bits) serial access memory (SAM). As this circuit incorporates the counter for address memory generation, the external address signal is not needed, and the address scan becomes the serial access. The internal address counter increments the address one by one from the clock pulse and is resets to zero address by the reset After data is written in address zero to 2047, the pulse. internal counter is reset to zero, and data is written.

Equivalent sampling pulse generator circuit

this circuit, refer to the EQV SPL section in Fig. 5-19, For and the timing chart Fig. 5-20. IC5302 is a 12-stage binary counter. This counter is COUNTER activated at the falling edge of the clock input (CK).

When

the clear input (CLR) goes high, the counter is reset regardless of the clock input, and all the outputs go low. The A SWEEP GATE signal form [73] is fed to CK. This gate signal is developed, based on the trigger signal in the RTO mode. Therefore, this counter is counted at each sweep. The counter output is converted into the analog signal by D/A RM5301, and fed to the (+) input terminal of COMPARATOR IC5304 via AMP IC5303. This (+) input voltage increases every sweep. On the other hand, the SWEEP RAMP signal as shown in Fig. 5-20 is fed to the (-) input terminal. When the SWEEP RAMP voltage exceeds the COMPARISON VOLTAGE fed to the (+) terminal, the "L" is output from the COMPARATOR. The COMPARATOR output is fed to $\langle 2 \rangle$ as the SH CLK via IC5306 (2/2) and the BUFFER & LEVEL CONVERTER. The rising edge of the SH CLK becomes a sampling point. In the BUFFER & LEVEL CONVERTER, a TTL level is converted into an ECL level. Whether the SH CLK is fed out or not is determined in IC5306 (2/2) by the EQ CKEN signal, which goes high in the equivalent sampling

mode.

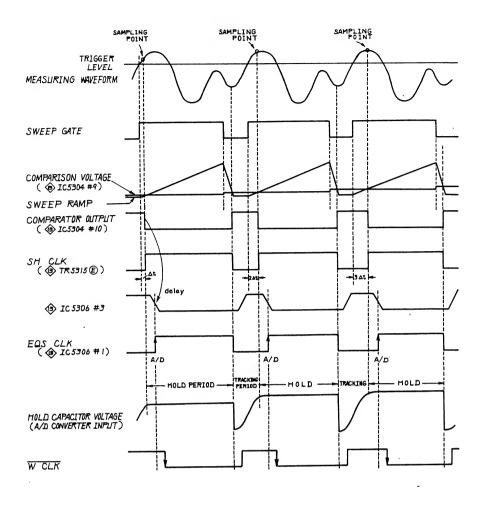


Fig. 5-20

EQUIVALENT SAMPLING

Part of the COMPARATOR output becomes the EQS CLK (equivalent sampling clock) via IC5314 (2/2) and IC5306 (1/2). In the equivalent sampling mode, the EQS CLK is fed to the CLK terminal of the A/D (1), and its rising edge performs the A/D conversion.

The A/D conversion is performed a little behind the sampling point by the delay circuit consisting of R5314 and C5409.

TBC and ACQ control circuit (Lower half of Fig. 5-19) The operation of this circuit is classified into 6 as listed in Table 5-4. (1) is the basic operation. Therefore, the differences from(1) are described in (2) to (6).

Operation mode	Sampling	Sampling clock freq.	Item	TIME/DIV	Remark
Equivalent sample	Equivalent sampling		(6)	50 ns - 2 μs	
Realtime sample	Realtime sampling	40 MHz	(4)	2.5 µs	VC-6045 only
		20 MHz	(3)	5 µs	
		10 MHz	(2)	10 µs	
		5 MHz - 1 kHz	(1)	20 µs - 0.1 s	Basic operation
ROLL		500 Hz-2 Hz	(5)	0.2 s - 50 s	

Table 5-4

(1) 20 μ s/div - 0.1 s/DIV

The 20 MHz pulse is always fed out from the terminal F of OSC X5301. The pulse obtained by dividing this pulse is fed out from the terminal D. The output frequency from the terminal D is changed according to the TIME/DIV range setting, and controlled by OSC's A, B and C. (Table 5-5)

TIME/DIV	OSCA	OSC B	OSC C	Terminal D output
50 ns - 2 µs				
2.5 µs - 0.1 s	L	L	L	10 MHz
0.2 s - 5 s	Н	Н	L	1.25 MHz
10 s	L	L	Н	625 kHz
20 s	Н	L	Н	312.5 kHz
50 s	Н	Н	Н	78.125 kHz

Та	bl	е	5	-5

COUNTER/TIMER IC5310 is a programmable counter/timer and has three 16-bit counters. The counter 0 (CLK 0, GATE 0 and OUT 0) is used as a divider, and the counter 1 (CLK 1, GATE 1 and OUT 1) is used as a pretrigger timer. The used counter is selected by A0 and A1.

Data is sent to D0 to D7 in three parts per processing.

1st ··· To which function data is used (counter or timer)
2nd ··· 8-bit data (including the dividing 16 bits
ratio per TIME/DIV setting) in total

3rd ••• 8-bit data

The maximum input frequency of COUNTER/TIMER IC5310 is 10 MHz, and its maximum output frequency is 5 MHz.

Consequently, the OSC output is fed to SELECTOR 2 IC5309 directly or via the counter 0 of the COUNTER/TIMER according to the TIME/DIV setting.

In case of the setting range from 20 μ s/DIV to 0.1 s/DIV, a 10 MHz pulse is fed out from the terminal D. This pulse is fed to the CLK 0 terminal of the COUNTER/TIMER, and the pulse divided in accordance with the TIME/DIV setting is fed out from the terminal OUT 0.

The output frequency of the terminal OUT 0 may or may not coincide with the sampling clock frequency. This is determined by the model number, single trace operation or dual trace operation, TIME/DIV range settings, etc.

The output from the terminal OUT 0 is fed to the 1B terminal of SELECTOR 1 IC5550, and further fed to the terminals 1C2 and 1C2 of SELECTOR 2 IC5309 from the terminal Y1.

The pulse fed to the terminal 1C2 is fed out from the terminal 1Y, resulting in the A/D1 CLK and the \overline{W} CLK1.

The pulse fed to the terminal 2C2 is fed out from the terminal 2Y, resulting in the clock which counts the number of sample.

The SELECTOR 2 is the switch which selects the desired

clock. The two sets of switches are switched similarly by the control signals CK SEL A and CK SEL B at the same time.

	CK SEL A	CK CEL B	Switch connection
20 MHz	L	L	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
10 MHz	Н	L	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Less than 5 MHz	L	Н	IC0 0 1Y 2C0 0 2Y IC1 0 2C1 0 2Y IC2 0 2C2 0 0 IC3 0 2C3 0 0
ES CLK (Equivalent sampling)	Η	Н	$\begin{array}{cccccccccccccccccccccccccccccccccccc$

Table 5-6

IC5316 (4/4) and IC5316(3/4) form the gate circuit. When pin 13 goes low, the clock fed to pin 9 passes this gate. This gate enters exclusive OR circuit IC5314 (4/4) at pin 10, and exclusive OR circuit (2/4) at pin 5. As pin 9 is the clock fed to pin 10 is fed out from pin 8 as low, is, resulting in the W CLK1. When the 40M ADC signal fed to pin 4 goes low, the clock fed to pin 5 is fed out from pin 5 as is, resulting in the WCLK2.

In this case, the WCLK1 and the WCLK2 are quite identical. When the 40M ADC signal is high, the clock fed to pin 5 is reversed and fed out from pin 6, resulting in the WCLK2. In this case, the phase of the WCLK1 is opposite to that of the WCLK 2.

The relationship between the A/D CLK and the A/D2 CLK is the same with that between the W CLK1 and the WCLK2.

Pin 12 of IC5315 (3/4)is low except for the ROLL mode. Consequently, the WCLK1 fed to pin 13 is fed out from pin as is, and fed to pin 2 of IC5312 (1/4) and pin 5 of 11 IC5312 (2/4). During the write period, as the ACQ1RD, IORD and ACQ2RD are all high, the WCLK1 is fed out from IC5312 (1/4) and IC5312 (2/4) as is, resulting in the R CLK1 and respectively. As described above, the write the RCLK2, clock and the read clock are identical during the write During the read period, the ACQ1RD, IORD and period. ACQ2RD go low at the respective timings. Consequently, the RCLK1 and the RCLK2 are controlled by IC5313 (2/3)and IC5313 (1/3), respectively. OE1 connects the ACQ MEM(1) to the data bus during the read period.

Next, the counter 1 (GATE1, CLK1 and OUT1) of COUNTER/TIMER IC5310, FF1 and FF2 are discussed below.

Normally, the contents of the ACQ memory is updated one by one according to the realtime sampling. However, it happens to stop the data update in the course of processing. For example, this happens when memory is reset or when the setting of TIME/DIV is changed.

When it is needed to stop updating data of the ACQ memory, the TRIG EN signal fed to D1 and R1 of FF 1 goes high. The rising edge of the GATE (A sweep gate) signal fed to

CK1 latches the signal, and the latched output is fed out from Q1. The Q1 output is synchronized to the write clock by FF2 and fed out from Q2.

When 1024 clocks enter COUNTER/TIMER IC5310 at CLK1 after the GATE1 input changes from low to high according to the Q2 output, the OUT1 output changes low to high. The clock frequency to CLK1 changes according to the TIME/DIV setting. While the OUT1 is low, the 1Y output of SELECTOR2 passes through gate IC5316 (3/4 and 4/4), and the write clock is supplied to the ACQ memory. When the OUT1 output goes high, pin 8 of IC5316 (3/4) is tied high, and the 1Y output of SELECTOR2 can not pass through gate IC5316 (3/4 and 4/4). Consequently, the write clock is not supplied to the ACQ memory, resulting in stopping the acquisition of data into the ACQ memory.

(2) 10 µs/DIV

In this case, the sampling frequency is 10 MHz and the 10 MHz pulse fed out from the terminal D of OSC X5301 is fed directly to SELECTOR2 IC5309. The other operations are the same with (1).

(3) 5µs/DIV

In this case, the sampling frequency is 20 MHz, and the 20 MHz pulse from the terminal F of OSC X5310 is fed directly to SELECTOR2.

FF3 and FF4 are the time measuring circuits, which are related to the 20M and 40M sampling. In case of the 20M sampling, the phase relation between the sampling clock and the ACQ trigger signal is checked according to the TRG 10M signal state, because the sampling capability and the count capability are different. Other operations are the same with (1).

(4) 2.5 µs/DIV (VC-6045 only)

In this case, the 40 MHz sampling frequency is required. However, the capability of the A/D converter is 20 MHz max. Consequently, two A/D converters are used, and the 40 MHz sampling is performed by reversing the phase of the A/D clock with respect to that of the other A/D clock.

Further, the relationship between the sampling clock and the ACQ trigger signal is checked from the status of the TRG 10 and the TRG 20M. The 40M ADC signal from OUTPUT PORT IC5307 is high.

(5) 0.2s/DIV - 50 s/DIV (ROLL mode)

When the TIME/DIV switch is set to this range, the ROLL

mode is automatically established. Each time when the ACQ memory acquires one data in the ROLL mode, the data is transferred to the buffer memory in the RAM. Thus, data is stored in the buffer memory during a specified duration. The number of the stored data changes in accordance with the TIME/DIV setting.

The data of the ROLL memory in the RAM is updated at a unit of the stored data amount. The ROLL memory facilitates the processing of waveforms in the ROLL mode. Later the display memory data in the same memory RAM is updated at a unit of the same data amount. When updating the ROLL memory and the display memory, data is shifted so that the oldest data is stored at the address 0.

Two display memories are provided for one channel. When the content of the first display memory is displayed on the CRT, the data of the second display memory is updated. During this time, the contents of the first display memory are displayed at a constant interval.

When the update of the second display memory finishes, the display memory changes from first to second, and the contents of the second display memory is displayed on the CRT. The same procedures are repeated between the two display memories.

The Write Enable Control (WECONT) signal goes high when acquiring data in the ACQ memory. When the WECTL signal goes high, the reset of FF5 and FF6 is released, and the Q6 output goes high. Pin 8 of IC5312 (3/4) is low even when the Q6 output goes high in the modes other than ROLL. Consequently, D7 of FF7 goes low, and INT ϕ goes high.

The output of the set-reset FF consisting of IC5316 (1/4.2/4) and IC5305 (2/5) is also low.

When the ROLL mode is established and the ROLL signal fed to pin 10 of IC5312 (3/4) goes high, pin 8 of IC5312 (3/4)

goes high. Consequently, D7 of FF7 goes high. When D7 goes high, the $\overline{INT \phi}$ signal remains high, and changes from high to low at the rising edge of the clock fed to CK7. The $\overline{INT \phi}$ signal is an interrupt signal. When the MPU for the DSO detects that the $\overline{INT \phi}$ goes low, the MPU issues the instruction "Read Data." According to this instruction, the ACQRD and \overline{IORD} go low. As a result, this output of pin 11 of IC5312 (4/4) goes low, FF7 is reset, and the $\overline{INT \phi}$ changes from low to high. Thus, the reading of one piece of data in the ROLL mode finishes. (6) 50 ns/DIV - 2 µs/DIV (Equivalent sampling mode)

- In this case, the EQS CLK fed out from pin 1 of IC5306 (1/2) is fed out from terminals 1Y and 2Y of SELECTOR 2 IC5309.
- (7) Channel selection in the storage mode (CKA and CKB signals) Refer to Fig. 5-21.

The channel selection in the RTO mode is performed by the $\overline{CH1}$ and $\overline{CH2}$ signals. In the storage mode, the channel selection is performed by the CKA signal. The channel selection of the A/D converter is performed by the CKB signal.

Two operating modes are available for the dual trace operation in the storage mode, and they are switched as follows according to the TIME/DIV range settings. (VC-6025 and VC-6045)

In the CHOP mode, the CHOP signal goes low, and 1Y and 2Y are connected to 1A and 2A, respectively, in SELECTOR 1

In the mode other than CHOP (including ALT), IC5500 (⟨1́3⟩). the CHOP signal goes high, and 1Y and 2Y are connected to 1B and 2B, respectively. As known from Fig. 5-21, the CKA is divided by 2 by IC2160 $(\langle 6 \rangle)$, and the outputs Q and Q become the CH2 DSP and CH1 DSP signals, respectively. In other words, the channel selection of the A/D input signal is performed by the CKA signal in the storage mode. The Q output also becomes the CKB signal, and becomes the AD clock in the CHOP mode. Fig. 5-22 illustrates the relationship among the CKA, CKB, AD clock and AD input signals.

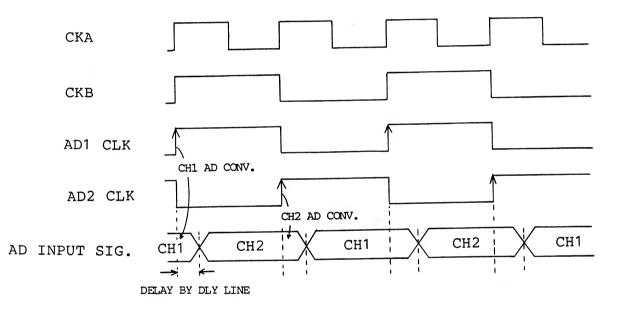
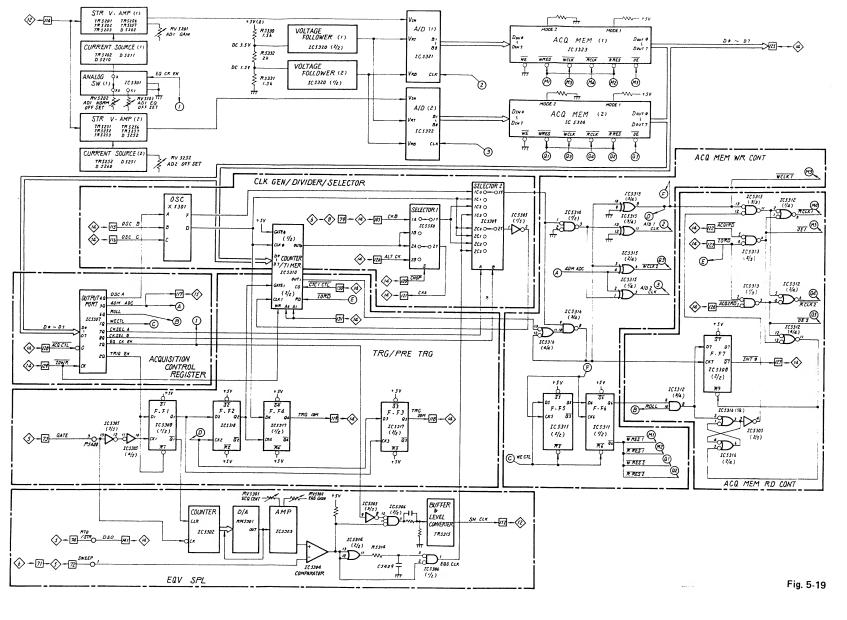


Fig. 5-22



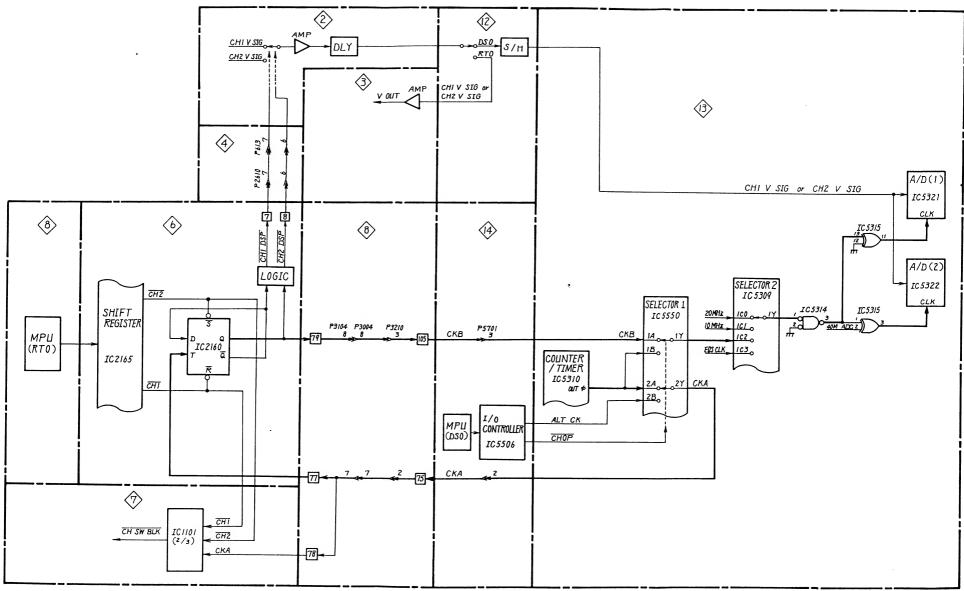


Fig. 5-21

5.14 Digital MPU ((14)) DISP CONT ((15) 1/2) FRONT PANEL (DSO) ((16))

For this circuit, refer to the detailed block diagram Fig. 5-23 of 14 and 16, the detailed block diagram Fig. 5-24 of 15 and the schematic diagram (14, 15 and 16) MPU IC5501 for the DSO of 14 is a CMOS 8-bit microprocessor, which has a high speed CPU, memory management unit (MMU), two direct memory access controllers (DMAC), timer, etc. The major functions of the MPU for the DSO include: (i) Display of data

- (ii) Control of the digital section
- (iii) Communications with the MPU for the RTO (transfer of data)
- (vi) Interface with external equipment

Control of display

The area of the buffer memory, the display memory, the save waveform memory, etc. are allotted in RAM IC5503 of (14).

The waveform data (2KB) is transferred from the ACQ memory to the buffer memory. Then the range 1KB to display one waveform data from the 2KB data by the H POS. This 1KB waveform data is transferred to the display memory.

One frame is approximately 20 ms. One frame includes the data of waveforms, characters, cursors, etc. The number of waveforms whose data is included in one frame is determined by operating modes (one channel, multi-channel, save mode, etc.). The maximum number of waveforms is four.

The display of one waveform is described in (1) to (3).

(1) Display in the Y direction of one waveform

The waveform data in the display region of RAM IC5503 of is fed out in sequence to OUTPUT CONTROLLER IC5518 of by the DMAC. The DMAC has the start and stop addresses of the display region. The DMAC generates addresses and updates the addresses successively (outputs the next address). The DMAC built in this MPU can transfer one data at 7 clock (0.8 µs approx.).

The MPU and the DMAC have the common data bus and address bus. Therefore, they uses the buses at the time division basis. In the instrument, the MPU and the DMAC use the buses alternately at every data transfer.

The MPU detects that the DMAC is requested when the DREC signal (DMAC Request) goes low and admits the use of the buses to the DMAC. Then, the DMAC lets the address bus to generate the start address, read one waveform data in the RAM, and transfer it to OUTPUT CONTROLLER IC5518.

(The start address is previously established in the DMAC.) The GATE 2 of TIMER IC5504 of 14 goes high every time when one waveform data is written in IC5518. When the GATE 2 goes high, the OUT 2 goes low. Consequently, the DREC goes high and the request to the DMAC is released. When the specified number of clocks is fed to the CLK 2, the OUT 2 goes back high. Accordingly, the DREQ goes low, and the DMAC is requested again. Then, the DMA cycle for the next waveform data output starts again.

The address is incremented every cycle.

The time between the data points is the sum of the DMA cycle (7 clocks), the count time of the TIMER 2 (GATE 2, CLK 2, OUT 2), and the reception time of the DREC. It is $3.2 \ \mu s \ approx$.

One waveform data is displayed by repeating the above processes until the stop address. (The stop address is also established previously in the DMAC.)

(2) Display of one waveform in the X direction

The MPU for the DSO incorporates two DMAC's : DMAC 0 and DMAC The display in the X direction is controlled by 1. DMAC 0 and that in the Y direction is controlled by DMAC 1. zero address of the display memory is selected to The be such an address that all of the lower 10 bits is zero. Thus, the D/A (2) output becomes the stairstep waveform that starts from zero volts.

The above 10-bit address is latched by the address latches LATCH 2 and LATCH 3 of (15). IC 5514 controls all the address (upper and lower addresses), and IC5512 controls the lower address. In case of the waveform display, both LATCH 2 and LATCH 3 perform the latch operation. The PC port of the OUTPUT CONTROLLER is in the input state by means of the MPU, and the signal is not output from the PC D/A (4). As described above, in case port to of the waveform display, the Y-direction signal is fed to D/A (1)the PA port of the OUTPUT CONTROLLER, from and the Xdirection signal is fed to D/A (2) from LATCH 2 and LATCH 3.

(3) Intensity control for the waveform display IC5514 (15)) controls the Z signal. In case of the waveform display, pins 10 and 11 of IC5514 are low. The DREQ signal fed to pin 9 continues to be low only for the time determined by the counter 1 (GATE 1, CLK 1, OUT 1) of TIMER IC 5504 (14). During this period, one piece of data is bright.

(4) X-Y operation

In this operation mode, the CH1 signal becomes the X signal, and the CH2 signal becomes the Y signal. Like the Y signal in the waveform display mode, the Y signal is fed to D/A (1) from the PA port of the OUTPUT CONTROLLER. The X signal is fed to D/A (4) from the DC port of the OUTPUT CONTROLLER. In this case, the outputs of LATCH 2 and LATCH

3 are in high impedance state and not connected electrically with D/A (4).

(5) Display of characters (Fig. 5-24)

One character consists of 3 bits each for the X and Y directions. The 3 bits in the X direction are output from terminals PB3 - PB5 of the OUTPUT CONTROLLER and converted into the analog signals by D/A (3). The 3 bits in the Y direction are output from terminals PB0 - PB1 and converted into the analog signals by D/A (2).

The number of the intensity bit which determines whether or not to brighten each for forming one character is one, which is output from terminal PB6.

As described above, 7 bits are used for one character. The character pattern for each character is stored in the ROM at the unit of 8 bits.

The characters of one upper row and two lower rows, 3 rows in total, are displayed on the CRT. The information on position in the Y direction which determines the position of one row is output from terminal PAO to PA7 and converted into the analog signal by D/A (1).

The 32 positions (5 bits) are set to display characters for The information on position in the X direction one row. which determines the 32 positions is determined by the 5 bits of the upper address fed out from LATCH 3 to D/A (4). this case, LATCH 2 is in the prohibit state. The D/A In (1) output whose voltage changes one time per row (every approx.) and the D/A (2) output whose voltage 2.5 ms every one dot (every 2 µs approx.) are added, changes resulting in the position signal in the Y direction.

Though the X direction of one screen consists of 10 bits (1024 points), the distance between two characters is $2^{10}/2^5 = 2^5$ (5 bits), because 32 characters (5 bits) are positioned with equal distance. In other words, the 5-bit point from the start point of the first character is the

start point of the second point. Consequently, the voltage of the D/A (4) output changes every $32 \times 2 \mu s = 64 \mu s$ approx. This D/A (4) output and the D/A (3) output whose voltage changes every one dot (every 2 μs approx.) and added, resulting in the position signal in the X direction.

(6) Cursor display (Fig. 5-24)

Like the character pattern, the cursor pattern is also stored in the ROM.

In case of the horizontal cursor, the position signal in the Y direction is constant and fed out from terminals PAO - PA7. Then the output signal is converted into the analog signal by D/A (1). The position signal in the X direction changes and is fed to D/A (4) from terminals PCO - PC7. The horizontal cursor consists of the 8-bit X-direction

signal.

In case of the vertical cursor, the Y-direction signal changes and is fed out to D/A (1) from terminal PAO - PA7. The position signal in the X direction is constant, and 10 bits are required according to waveform. The 10 bits are output from LATCH 2 and LATCH 3 and converted into the analog signal by D/A (4). As described above, the instrument does not require a conventional cursor pattern generator. Consequently, the number of bits is reduced to a minimum, and an affective operation is ensured.

ANALOG SW, MULTIPLEXER (Fig. 5-24)

The switches X and Y of ANALOG SW are controlled by the DOTj signal, and the smooth on-off switching is made. The signal passes LPF at the time of the smooth on. "Smooth on" or "smooth off " is displayed on the screen by switching the MENU switch at the lower left of the front panel. The switch Z of ANALOG SW (2) is controlled by the 40M ADC signal and the gain of MULTIPLEXER (2) is switched.

MULTIPLEXER is controlled by the DSO signal, and the signal

flow is changed according to the RTO mode or the DSO mode. In case of the RTO, the output of the operational amplifier A in each MULTIPLEXER becomes the CHST-Y and CHST-X signals. In case of the DSO, the output of the operational amplifier B in each MULTIPLEXER becomes the CHST-Y and CHST-X signals. The Y-direction signal of characters and cursors or the A/B SEP BIAS signal in the RTO mode is fed to the operational amplifier A of MULTIPLEXER (1). While, the Y-direction signal of waveforms, characters and cursors in the DSO mode is fed to the operational amplifier B.

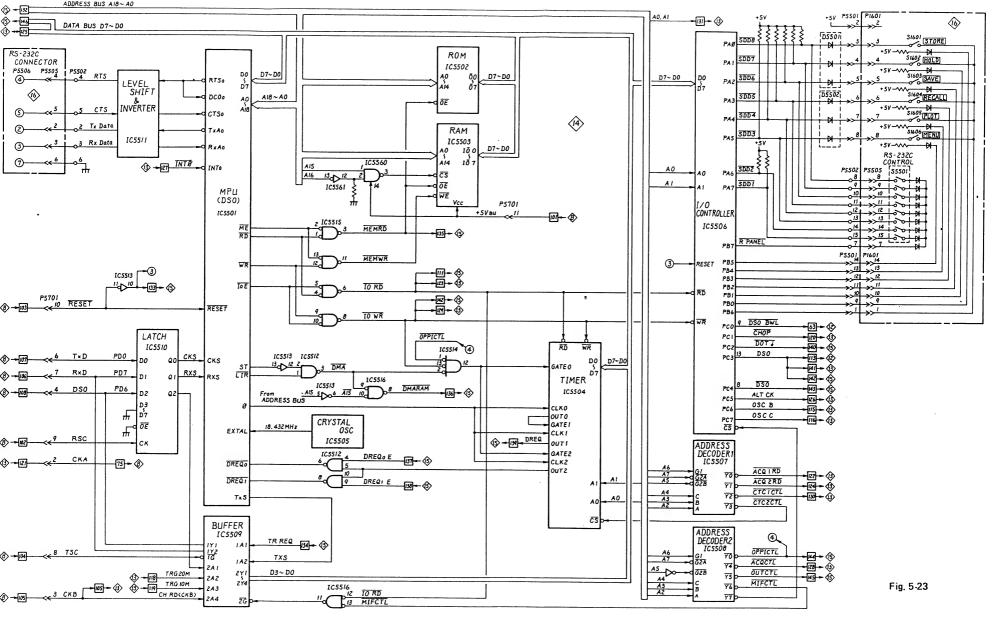
The X-direction signal of characters and cursors in the RTO mode is fed to the operational amplifier A in MULTIPLEXER (2). The X-direction signal of waveforms, characters and cursors is fed to the operational amplifier B.

Control of the DSO switch and RS-232C CONTROL switch (Fig. 5-23) The descriptions of the 6 DSO switches (S1601 - S1606) at the lower left of the front panel and the 8-circuit DIP switches on the rear follow.

As known from terminals PAO - PA5 of I/O CONTROLLER IC5506, the status of the two switches can be judged by one line. In other words, the status of the DSO switch and the DIP switch is checked by the MPU for the DSO at some sequence.

When checking the status of the DSO switch, the MPU make the R PANEL signal high and PB6 low. Under this condition, all the switches of S5501 are the same as the off state when viewed from PA terminal side regardless of their actual setting positions.

Consequently, only the PA terminal corresponding to the on switch goes low. Thus, the MPU judges the switch that is on. Later, the MPU make the corresponding terminal among PBO thru PB5 low, and the LED corresponding to the pressed switch. When checking the DIP switches, the MPU makes the R PANEL signal low and PB6 high. The operation is identical with the DSO switch.



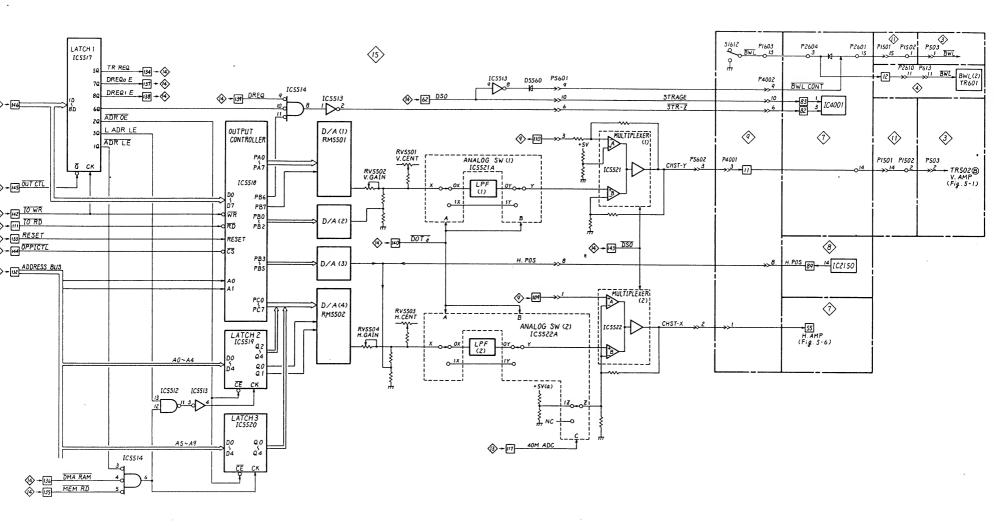
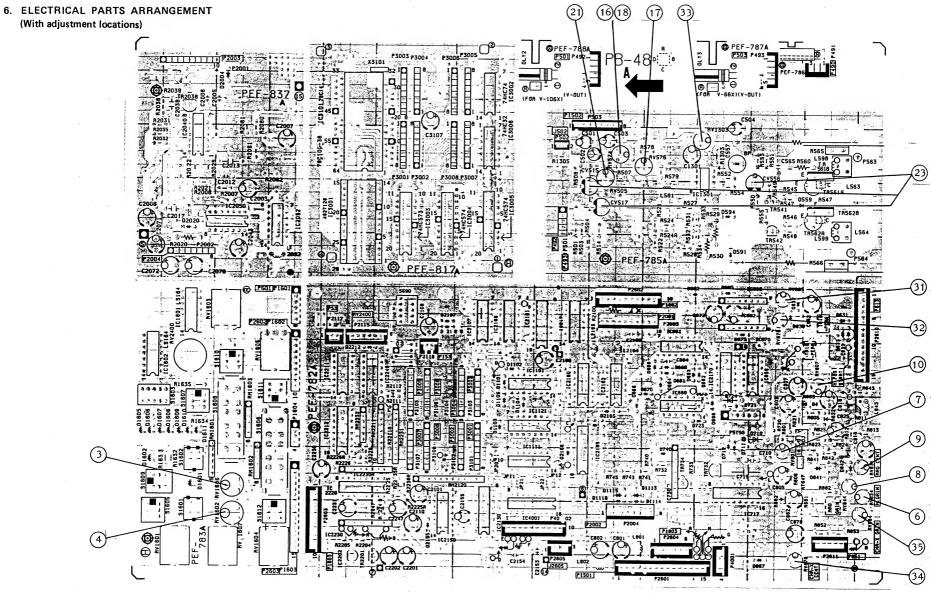
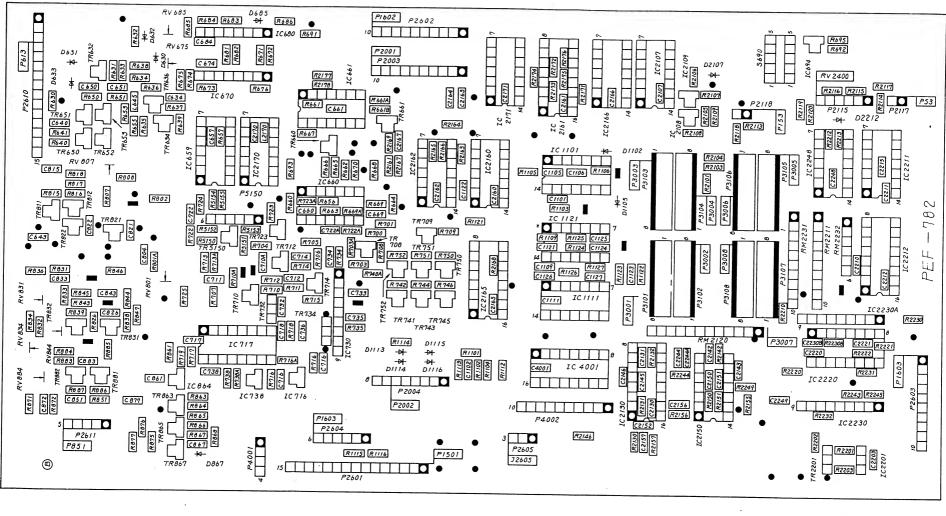


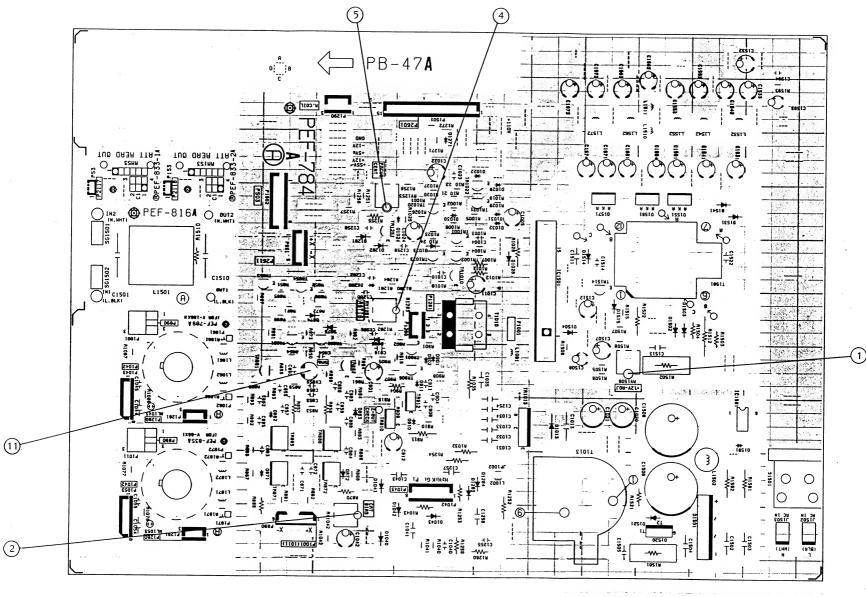
Fig. 5-24



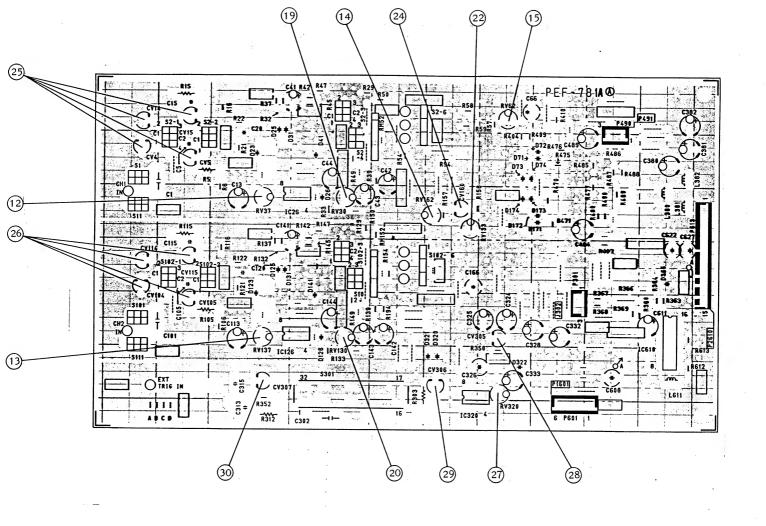
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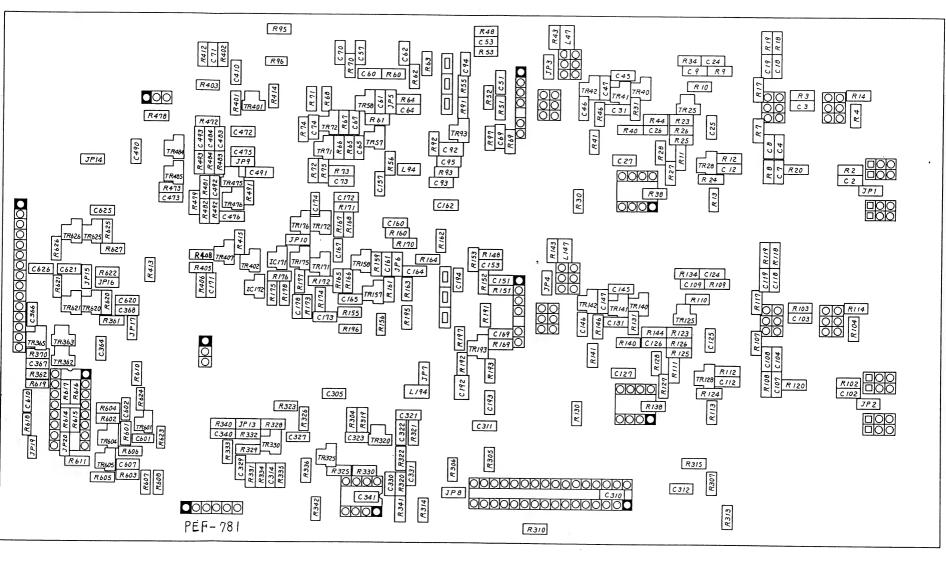
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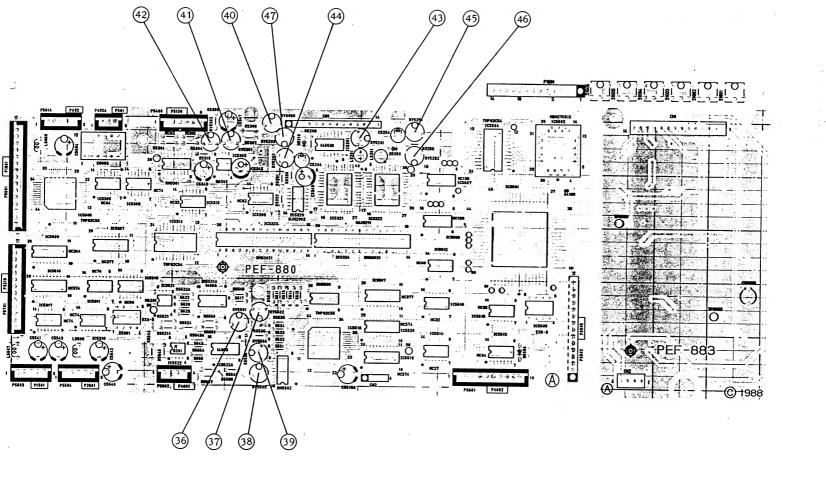
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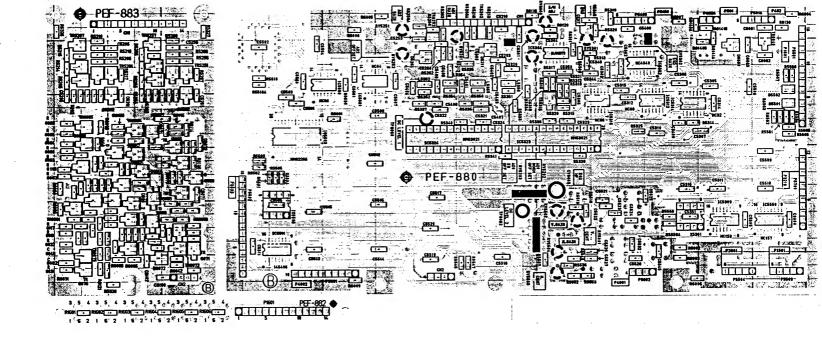


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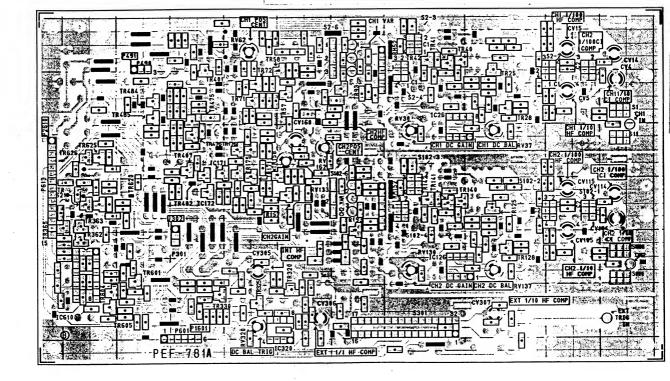


PEF-781 (Soldering side)

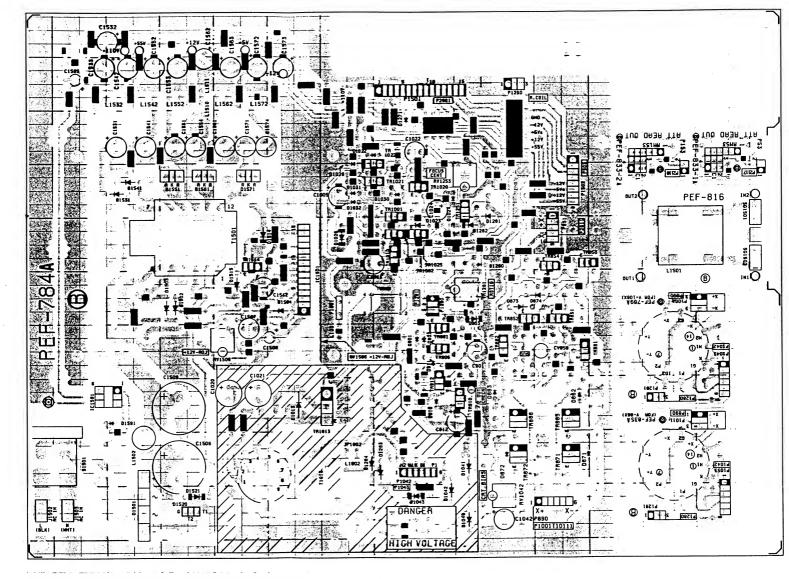




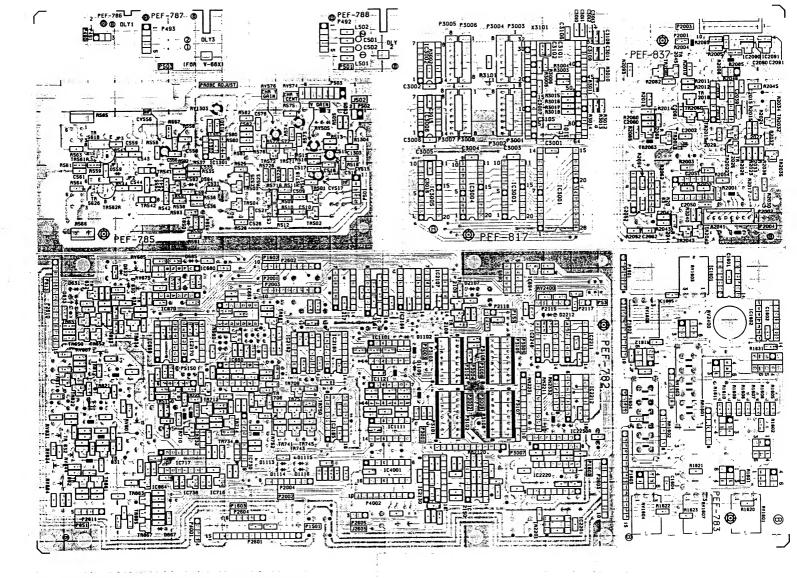
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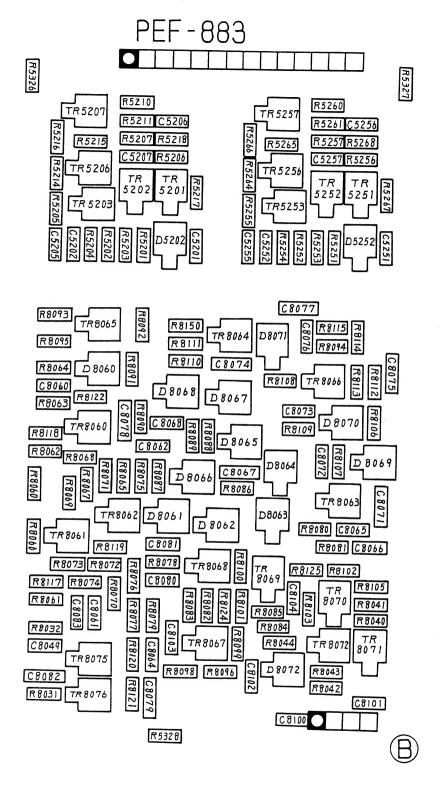
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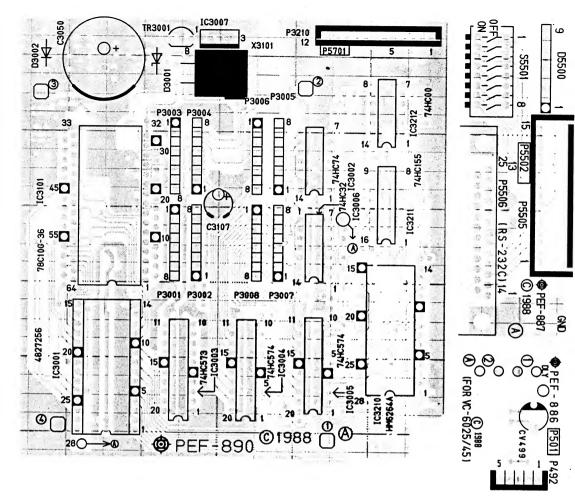
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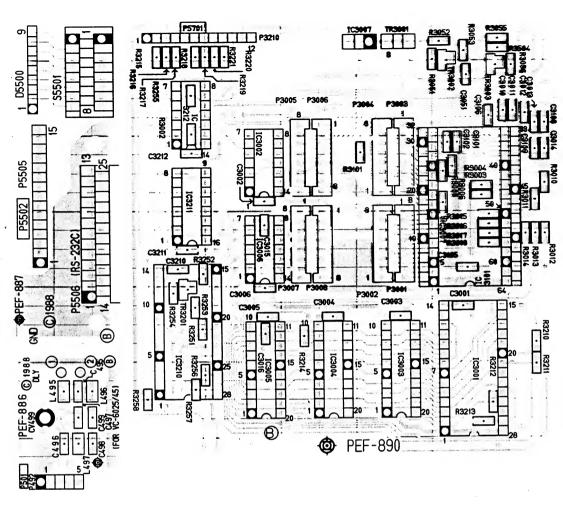
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PEF-883 (Soldering side)

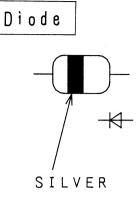


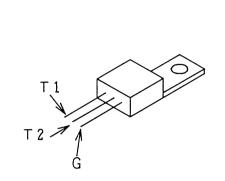
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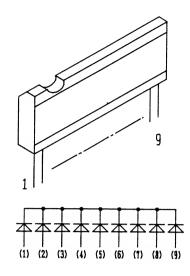


PEF-886, 887, 890 (Soldering side)

7. ELECTRICAL PARTS LEAD CONFIGURATIONS



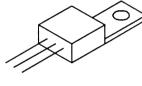


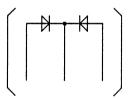


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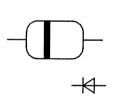
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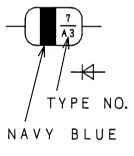




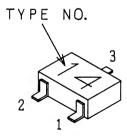
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GZB 2.4B GZB 3.0B GZB 6.8B

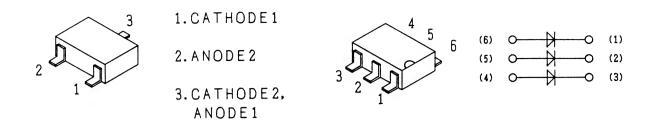


HZ7A1 HZ7A3



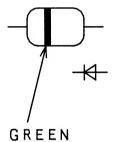
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3.CATHODE	ТҮРЕ	NO.24	ΗΖМ	7 C

HZM SERIES

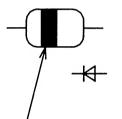


HSM88S

IMN10

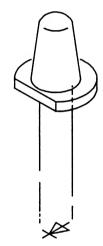


MA161

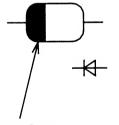


CATHODE BAND

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1 S S 1 2 3	MTZ SERIES
1 S S 1 3 3	
1 S S 1 5 3	

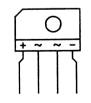


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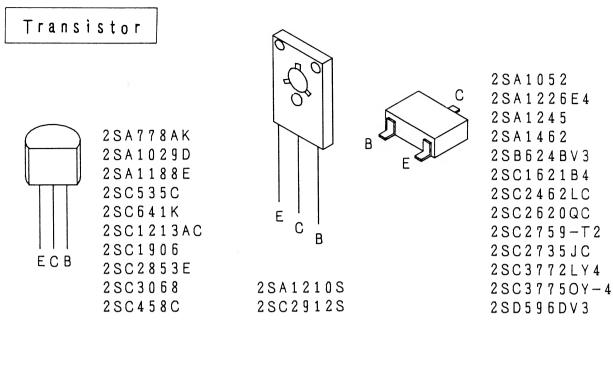


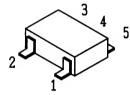
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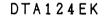
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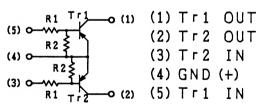


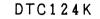
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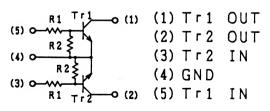


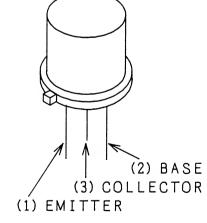




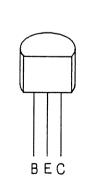




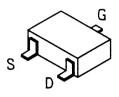




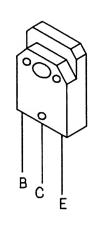
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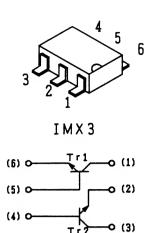
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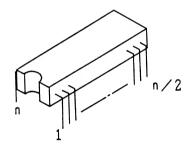
2 S K 3 0 3 V 4 2 S K 4 3 6 A 2 0 2 S K 5 0 8 K 5 2



2SC3089







8	Ρ	I	N	S	
MN	3	1	0	2	

1	4	Ρ	I	N	S	
				_		_

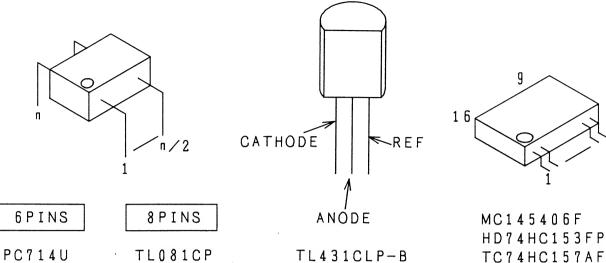
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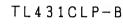
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HD14051BP							
HD14053BP							
HD74HC138P							
H D 7 4 H C 1 5 5 P							
H D 7 4 H C 4 0 4 0 P							
HD74LS157P							
MC10H116L							
MC74HC4052N							
MC74HC4053N							
SN 7 4 L S 5 9 4 N							
TC40H151P							

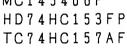
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28PINS
H N 2 7 2 5 6 G – 2 H M 6 3 0 2 1 P
64PINS

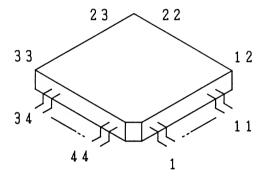
5

µPD78C10G-36



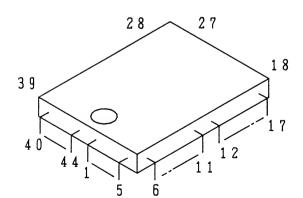




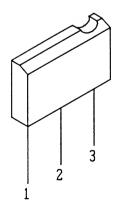


13 24 12 1

TMP182C55AF-10



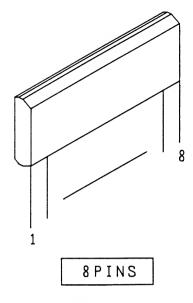
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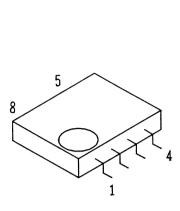
1. Vss 2. V dd 3. OUT

HA19211MP

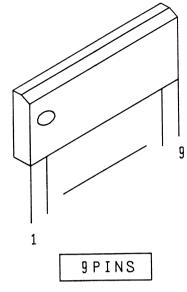
MN1280R



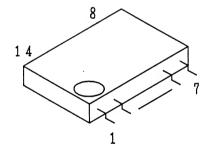
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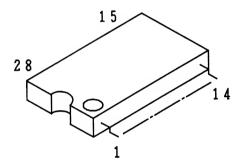




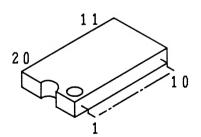
NJM072S



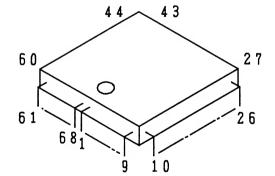
N J M 3 1 9 M N J M 2 9 0 2 M H D 7 4 H C 2 7 F P H D 7 4 H C 3 2 F P T C 7 4 H C 0 0 F T C 7 4 H C 8 6 F



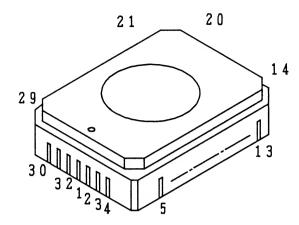
HM 6 2 2 5 6 L P F - 1 0 T HM 6 2 6 4 A L P - 1 5



HD74HC377FP TC74HC244F TC74HC574AF



HD64180R1CP10



MBM27C512-20 (LCC)

8. ELECTRICAL PARTS LIST V-PRE & TRIG AMP (PEF-781)

A : VC-602	5 3 : VC-604		-781 V-PREETRIG AMP		VC-6025			-781 V-PRESTRIG AMP	J Q.TY
C 1 C 1 C 2 C 3 C 3 C 3 C 3 C 3 C 3 C 3 C 3 C 3 C 3		C.PLASTIC C.PLASTIC C.CERAMIC	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	x 1 1 25PF 1 1 25PF 1 1 -0X 1 1 SPF 1 1 -0X 1 1 SPF 1 1	 $\begin{array}{c} \text{JOL} \\ JOL$		C.AL ELVC C.AL ELVC C.AL ELVC C.CERAMIC C.CERA	<pre>JESCR PTION 10 V 470 UF20x 14 V 300 UF20x 50 V 1000 UF20x 50 V 7000 PF0.3PF 50 V 7 PF0.3PF 50 V 7 PF0.3PF 50 V 7 PF0.3PF 50 V 100 PF0.3PF 50 V 100 PF0.3PF 50 V 100 PF0.3PF 50 V 22000 PF20x 50 V 22000 PF20x 50 V 2000 PF20x 50 V 100 PF20x 50 V 1000 PF10x 50 V 1000 PF10x</pre>	
A : VC-6025	5 B · VC-604								
A : VC-6C25 SYHBOL C 120 C 122 C 122 C 122 C 122 C 127 C 131 C 142 C 142 C 143 C 144 C 146 C	B : VC-604 PART C00E CC00284 CC00214 CC00214 CC60214 CC60214 CC602114 CC602114 CC602114 CC602114 CC60211 CC60213	······································	ZB1 V-PREATRIG AMP SIGN PTION	1 1 1 1	124 1141 1141 1142 1177 1176 1177 1177 1177 1177 1177 117	B : VC-604 PART CODE HDS0677 HDS0677 HDS06477 HDS06477 HDS06477 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HDS06437 HT00161 LT00161 LT00161 IDM0162 RME0912 RME0002 RME0912 RME0002 RME0912 RME0002 RME000 RME000 RME0000 RME0000 R		ZAL V-PRELTRIG AMP ESCRIPTION	

: VC-6025 B : VC		PEF-781 V-PRESTRIG AMP	1 Q.TY].	A : VC-602		1	PEF-781 V-PREETRIG AMP	
BOL PART CO	E	DESCRIPTION	A B	SYMBOL	PART CODE	R.METAL	DESCRIPTION	î
6 RME1163	R.METAL	1/4W 111 KOHM +-0.5%		R 144	RME0862	RIMETAL	1/4W 475 OHM +-0.5X	1
7 RME0865	R.METAL	1/8W 120 0HM +-5%	1 1 1 1	R 145	RME1595 RME0878	R.METAL	1/8W 1.5 KOHM +-5X	1
8 RME0858	R.METAL	1/8W 33 OHM +-5%		R 146		R.METAL	1/4W 22.1 OHM +-0.5%	1
9 RME0873	R.METAL	1/8W 560 0HM +-5%	1 1 1 1	R 147	RME 1663 RME0868	R.METAL	1/8W 220 OHM +-5x	1
10 RME0852	R.METAL	1/8W 10 OHM +-5X		R 148	RME1157	R. METAL	1/4W 16.0 KOHM +-0.5%	1
11 RME0864	R.METAL	1/8W 100 0HM +-5x	1 1 1 1	R 149 R 150	RME 1596	R.METAL	1/4W 24.0 KOHM +-0.5%	1
12 RME0888	R.METAL	1/8W 10 KOHM +-5x		R 151	RME0870	R.METAL	1/8W 330 OHM +-5%	1
13 RME0891	R.METAL	1/8W 18 KOHM +-5X 1/8W 12 DHM +-5X	1 2 2 1	R 152	RME0870	R.METAL	1/8W 330 OHM +-5X	1
14 RME0853	R.METAL			R 153	RME0865	R.METAL	1/8W 120 OHM +-5X	1
15 RMS0044	R.METAL		1 1 1 1	R 154	RME1195	R.METAL	1/4W 110 KOHM +-1%	1
16 RME1156	R.METAL			R 155	RME0900	R.METAL	1/8W 100 KOHM +-5X	1
17 RME0866	R.METAL	1/8W 150 0HM +-5% 1/8W 10 0HM +-5%		R 156	RME0888	R.METAL	1/8W 10 KOHM +-5%	1
18 RME0852	R.METAL R.METAL			R 157	RME1077	R.METAL	1/4W 2.67KOHM +-1%	1
19 RME0851	R.METAL	1/8₩ 6.8 0HM +-10% 1/4₩ 500 K0HM +-0.5%		R 158	RME 1077	R.METAL	1/4W 2.67KOHM +-1%	1
21 RME1168	R.METAL	1/4W 500 KOHM +-0.5X	1 4 4 1	R 159	RME0863	R.METAL	1/8W 82 OHM +-5X	1
22 RME1168	R.METAL		1 1 1	R 160	RME0868	R.METAL	1/8W 220 0HM +-5%	1
23 RME1597	RIMETAL			R 161	RME0876	R.METAL	1/8W 1.0 KOHM +-5%	
24 RME0876			1 1	R 162	RME0892	R-METAL	1/8W 22 KOHM +-5%	1
25 RME0860	R.METAL			R 163	RME0883	R.METAL	1/8W 3.9 KOHM +-5%	1
26 RME0868	R.METAL R.METAL		1 1 1 1	R 164	RME0862	R.METAL	1/8W 68 OHM +-5%	1
27 RME0886				R 165	RME0854	R.METAL	1/8W 15 OHM +-5%	1
28 RME0877	R.METAL			R 166	RME 0869	R.METAL	1/8W 270 0HM +-5%	1
29 RME1591	R.METAL R.METAL			R 167	RME0854	R.METAL	1/8W 15 OHM +-5%	1
30 RME0888				R 168	RME0869	R.METAL	1/8W 270 0HM +-5%	1
31 RME0852	R.METAL R.METAL			R 169	RME0912	R.METAL	1/8W 0 0HM	1
31 RME0856			1	R 170	RME0863	R.METAL	1/8W 82 OHM +-5X	1
33 RME1081	R.METAL			R 171	RMED860	R.METAL	1/8W 47 OHM +-5%	1
34 RME0892	R.METAL			R 172	RME0861	R.METAL	1/8W 56 OHM +-5%	1
37 RME1662	R.METAL			R 173	RME0860	R.METAL	1/8W 47 0HM +-5X	1
38 RME0897	R.METAL			R 174	RMEOB88	R.METAL	1/8W 10 KOHM +-5%	1
39 RCE0768	R.CARBO		1	R 175	RMEO888	R.METAL	1/8W 10 KOHM +-5%	1
40 RME0880	R.METAL			R 175	RME0882	R.METAL	1/8W 3.3 KOHM +-5%	1 1
41 RME0864	R.METAL		1	R 177	RME0861	R.METAL	1/8W 56 OHM +-5X	1
42 RME1661	R.METAL		1 1	R 178	RME0860	R.METAL	1/8W 47 OHM +-5X	1
43 RME0864	R . METAL			R 191	RME0861	R.METAL	1/8W 56 OHM +-5X	1
44 RME0862	R.METAL			R 192	RME0863	R.METAL	1/8W 82 0HM +-5x	1
45 RME1595	R.METAL		1	R 193	RME0864	R.METAL	1/8W 100 0HM +-5%	1 1
46 RME0878	R.METAL R.METAL		1 1	R 194	RCE0770	R.CARBON	1/4W 1.2 KOHM +-5%	1
47 RME1663			1 1 1 1	R 195	RME0864	R.METAL	1/8W 100 0HM +-5%	1
48 RME0868	R.METAL			R 196	RME0883	R.METAL	1/8W 3.9 KOHM +-5X	1 1
49 RME1157	R.METAL			R 303	RMS0049	R. METAL	1/2W 1 MOHM +-0.5%	1 1
50 RME1596	R.METAL		1 1 1	R 304	RME0874	R.METAL	1/8W 680 OHM +-5%	1 1
51 RME0870	RIMETAL			R 305	RME0861	R.METAL	1/8W 56 OHM +-5%	1
52 RME0870	R.METAL			R 305	RME0861	R.METAL	1/8W 56 OHM +-5%	1 1
53 RME0865	R.METAL			R 307	RME0870	R.METAL	1/8W 330 OHM +-5%	1 1
54 RME1195	R.METAL		1	R 310	RME0876	R.METAL	1/8W 1.0 KOHM +-5X	1 1
55 RME0900	R.METAL			R 312	RMS0043	R.METAL	1/4W 900 KOHM +-0.5%	1 1
56 RME0888	R.METAL	1/8W 10 KOHM +-5%	1 1	R 313	RME0872	R.METAL	1/8W 470 DHM +-5X	1 1
57 RME1077	R.METAL			R 314	RME0875	R.METAL	1/8W 820 0HM +-5%	1 1
58 RME1077	R.METAL				RME0852	R.METAL	1/8W 10 0HM +-5%	1 1
59 RME1057	R.METAL			R 315 R 319	RME0884	R.METAL	1/8W 4.7 KOHM +-5%	1 1
60 RME0866	R.METAL			R 320	RME0906	R.METAL	1/8W 1.0 MOHM +-5%	1
61 RME0876	R.METAL			R 321	RME0867	R.METAL	1/8W 180 0HM +-5%	1 1
62 RME0892	R.METAL			R 322	RME0860	RIMETAL	1/8W 47 OHM +-5%	1 1
63 RME0883	R.METAL		14 41	R 323	RME0876	R.METAL	1/8W 1.0 KOHM +-5X	1 1
64 RME0862	R.META	1/8W 68 OHM +-5X	1	R 323		1		1
						1		1
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SWP LOGIC (PEF-782)

A : VC-60	25 3 : VC-604	5 PE	F-781 V-PREATRIG AMP	SWP LO	
SYMBOL R 489 R 490 R 492 R 492 R 493 R 493 R 601 R 602 R 603 R 605 R 605 R 605 R 605 R 615 R 611 R 615	PART CODE RHE 10/72 RHE 10/72 RHE 08/63 RHE 08/64 RHE 08/64 RHE 08/64 RHE 08/64 RHE 08/64 RHE 08/64 RHE 08/64 RHE 08/64 RHE 08/62 RHE 08/62 RHE 08/72 RHE 08/72 RHE 08/72	R.METAL R.METAL R.METAL R.METAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL	DESCRIPTION	 A : VC-602 SYMBOL 6 7 12 14 16 17 C 630 C 632 C 634 C 640 C 64	5 E # F E T F E T F E T F E T F C
R 616 R 617 R 617 R 627 R 629 R 629 R 629 R 622 R 622 R 622 R 622 R 622 R 622 R 622 R 622 R 7 R 627 R 152 R 7 R 152 R 7 R 133 R 7 R 133 R 7 R 132 R 7 R 133 R 7 R 132 R 133 R 135 R 133 R 135 R	R HE 0.8 7 4 R HE 0.8 7 4 R HE 0.8 6.3 R HE 0.8 6.3 R HE 0.8 5.2 R HE 0.8 7.3 R HE 0.0 4.7 R	R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL R.HETAL VR.HETAL VR.HETAL VR.HETAL VR.HETAL VR.HETAL VR.HETAL	1/84 680 0HH +-5% 1/84 680 0HH +-5% 1/84 82 0HH +-5% 1/84 82 0HH +-5% 1/84 18 0HH +-5% 1/84 18 0HH +-5% 1/84 540 0HH +-5% 1/84 540 0HH +-5% 1/84 540 0HH +-5% 1/84 18 00HH +-5% 1/84 10 0HH +-5% 1/84 10 0HH +-5% 1/84 470 K0HH +-5% EXB-087059FNP EXH-39C00YB54(50K) EVH 39C00YB54(50K) EVH 39C00YB54(50K) EVH 39C00YB54(50K) EVH 39C00YB54(50K)	C 669 C 672 C 674 C 682 C 710 C 710 C 711 C 711 C 712 C 715 C 715 C 722 C 722 C 733 C 733 C 735 C 736 C 738 C 738	
RV 320 S 1 S 101 S 102 S 111 S 301 TR 25 TR 26	R ME 0047 SSP0574 S4728134 S5P0574 S472813 0 S5P0574 S5P0574 S5P0574 S5P0574 HTC0871	VR. METAL SU., ROTARY SU., ROTARY SU., ROTARY SU., ROTARY SU., ROTARY SU., ROTARY SU., ROTARY TRANSISTOR TRANSISTOR	EVN 39C00Y854(50K) SPUJ-1 ADR235518711PY02(W.85.GND SPUJ-1 ADR255188711PY02(W.S5.GND SPUJ-1 SR254 25K308K52/25K508K52NV 25C3772LY4	C 802 C 804 C 804 C 807 C 817 C 813 C 815 C 815 C 822 C 825 C 825 C 826	CES CES CES CES CES CES CCG CCG CCG

	4.TY	A : VC-6025 B : VC-60	45 PEF-782 SWP LOGIC R : Not used	
м м м		A.: VC-6025 B.: VC-60 SYMBOL PART CODE 4 EIP0141 12 ETP0141 14 ETP0141 15 ETP0141 16 ETP0141 17 ETP0141 17 ETP0141 17 ETP0141 17 EC0231 17 EC0201 17 EC0211 17 CC00211 17 CC00211 17 CC00211 17 CC00211 17 CC00211 17 CC00211	R : Not used	B 1 1 1 1 1

A : VC-6025 B : VC-604	5 PEF-781 V-PRESTRIG AMP		A : VC-602	5 B : VC-604	5 PEF	-782 SWP LOGIC	
A : VC-6025 B_: VC-6045 SYMBOL PART CODE TR 40 HTA0334 TR 41 HTC0871 TR 41 HTC0871 TR 41 HTC0871 TR 54 HTC0871 TR 71 HTC0871 TR 72 HTC0871 TR 73 HTC0871 TR 74 HTC0871 TR 74 HTC0871 TR 75 HTC0871 TR 140 HTA0318 TR 141 HTC0871 TR 153 HTC0871 TR 154 HTC0871 TR 152 HTC0871 TR 152 HTC0871 TR 153 HTC0871 TR 154 HTC0871 TR 155 HTC0871 TR 350 HTC0871 <td>S PEF-T81 V-PRELTRIG AMP TRANSISTOR DESCRIPTION </td> <td> G. TY 1 1 1 1 1 1 1 1 1 1 1 1 1</td> <td>A : VC-602 SYMBOL C 843 C 843 C 843 C 841 C 842 C 1001 C 1102 C 1105 C 1105 C 1106 C 1107 C 1112 C 1127 C 2100 C 2107 C 2107 C 2107 C 21127 C 2144 C 2144 C 2145 C 2145 C 2155 C 2155 C</td> <td>PART CODE CCG0211 CCG01431 CCG01431 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0199 CCG0199 CCG0199 CCG0199 CCG0199 CCG0199 CCG0211 CCG0296 CCG0296 CCG0296 CCG0213 CCG0213 CCG0211 CCG0205 CCG0213 CCG02213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0221 CCG0211 CCG</td> <td>C.CERAMIC C.CERAMIC</td> <td>-782 SWP LOGIC R , Not used</td> <td> 0.19 0.19 R R </td>	S PEF-T81 V-PRELTRIG AMP TRANSISTOR DESCRIPTION	G. TY 1 1 1 1 1 1 1 1 1 1 1 1 1	A : VC-602 SYMBOL C 843 C 843 C 843 C 841 C 842 C 1001 C 1102 C 1105 C 1105 C 1106 C 1107 C 1112 C 1127 C 2100 C 2107 C 2107 C 2107 C 21127 C 2144 C 2144 C 2145 C 2145 C 2155 C	PART CODE CCG0211 CCG01431 CCG01431 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0199 CCG0199 CCG0199 CCG0199 CCG0199 CCG0199 CCG0211 CCG0296 CCG0296 CCG0296 CCG0213 CCG0213 CCG0211 CCG0205 CCG0213 CCG02213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0213 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0221 CCG0211 CCG	C.CERAMIC C.CERAMIC	-782 SWP LOGIC R , Not used	0.19 0.19 R R
TR 601 HTA0318 TR 604 HTC0872 TR 605 HTC0872 TR 620 HTC0872 TR 621 HT0334 TR 625 HTA0334	TRANSISTOR 25A1462Y34 TRANSISTOR 25C26200C TRANSISTOR 25C26200C TRANSISTOR 25C26200C TRANSISTOR 25A1226E4 TRANSISTOR 25A1226E4		C 2151 C 2152 C 2153 C 2154 C 2155 C 2155 C 2156 C 2157	CCG0213 CCG0211 CQE0062 CQE0062 CEK0186 CCG0124	C.CERAMIC C.CERAMIC C.PLASTIC C.PLASTIC C.AL ELYC C.CERAMIC	50 V 0.1 UF+80-20X 50 V10000 PF+-10X 50V 1MF +-5X 50V 1MF +-5X 50 V 4.7 UF+-20X 50 V 10 PF+-0.5PF	

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0610	68 -68 -68 -68 -68 -68 -68 -4 -4	
EF-782 SWP L	BBP-SHF BBP	
5 P	CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR R.HETAL	S
B : VC-604		5 B • VC-604 . PART CODE RHE 0880 RHE 0856 RHE 0856 RHE 0856 RHE 0856 RHE 0857 RHE 0868 RHE 0867 RHE 0868 RHE 0858 RHE 08588 RHE 08588 RHE 08588 RHE 08588 RHE 08588 RHE 08588 R
A : VC-602	SV PP 31004 PP 31004 PP 31006 PP 31006 PP 31006 PP 31006 PP 5 6 301 SV 66323 SV 6632 SV 66323 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 6632 SV 8 SV 8 SV 8 SV 8 SV 8 SV 8 SV 8 SV	A : VC-602 SYM60L R 691 R 692 R 7003 R 7003 R 7003 R 7003 R 7003 R 7003 R 7003 R 7005 R 7100 R 7105 R 715 R 715
1.1.1.1		. 0.17
		0P BCP BCP 20X 7UH) 7UH) H10X H10X
782 SWP LOGIC	DESCRIPTION 50 V10000 PF- 50 V10000 PF- 50 V10000 PF- 50 V10000 PF- 50 V10000 PF- 50 V10000 PF- 50 V10000 PF- 16 V 47 UF- 16 V 47 UF- 50 V10000 PF- 50 V10000 PF-	SN74ASDDN SN74ASDDN SN74AS74C00P/TC74HC00 MISSOIL 01A124EK DIC124EK DIC124EK DIC124EK DIC124EK HC74HC4053N HC74HC4053N HC74L510P HC74L500P HC74L500P HC74L500P HC74L500P HC74L50P HC74L5374P TC40H151P HC74L5374P TC40H02P HC74L5374P TC40H02P HC74L5374P TC40H02P HC74L5373P HC74L5374P TC40H002P HC74L5374P TC40H002P HC74L537P EL06065KI 1F0K C22UH 450 MA +-2 EL06075KI 470K 47 EL06075KI 470K 47
5 PEF		
5 B : VC-604	PART CODE CCG0211 CCG021	PART CODE ID50444 ID50445 ID50445 ID50445 ID5045 ID5045 ID5045 ID5045 ID5045 ID5045 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50447 ID50445 ID5045 ID504
A : VC-602	SYMBOL C 2203 C 22201 C 2221 C 2221 C 2221 C 22221 C 22221 C 22221 C 22221 C 22221 C 22221 C 22221 C 22221 C 22221 C 2224 C 224 C 224 C 224 C 224 C 2245 C 2	A : VC-602 SYMBOL IC 6659 IC 661 IC 6700 IC 710 IC 710 IC 7138 IC 710 IC 717 IC 717 IC 710 IC 717 IC 710 IC 717 IC 710 IC 710

A : VC-6025	5 B : VC-604	5 PEF-7	82 SHP LOGIC	-	A : VC-60	25 B · VC-604	5 00	5 742 AUD - 4444	
SYMBOL R 8004 R 8004	PART CODE RME1412 RME1412 RME161073 RME1073 RME1073 RME1073 RME1073 RME1074 RME1074 RME1074 RME1074 RME1074 RME1074 RME1074 RME1074 RME1074 RME1074 RME1074 RME1074 RME0876 RME0876 RME0876 RME0876 RME0876 RME0876 RME1078 RME1078 RME1078 RME1078 RME1078 RME1078 RME0876 RME0	DE R.HETAL R	1/44 4.32KOHM11 1/44 4.32KOHM12 1/44 1.21KOHM12 1/44 1.21KOHM12 1/44 6.1 OHH12 1/44 4.1 OHH12 1/44 2.43KOHM12 1/44 2.43KOHM12 1/44 2.43KOHM12 1/44 2.43KOHM12 1/44 3.0 KOHM52 1/44 3.0 KOHM52 1/44 1.50KOHM12 1/44 1.0 KOHM52 1/44 22 OHM12 1/44 22 COHM12 1/44 22 COHM12 1/44 22 KOHM12 1/44 20 KOHM52 1/44 20 KOHM52	A. B. YY. A. B. J.	A : VC-60. SVH80L R 2175 R 2177 R 2177 R 2177 R 2177 R 2207 R 2203 R 2203 R 2203 R 2203 R 2203 R 22111 R 2213 R 2211 R 2213 R 2223 R 2224 R 2223 R 2223 R 2223 R 2223 R 2223 R 2223 R 2223 R 2224 R 2223 R 2223 R 2224 R 2223 R 2223 R 2224 R 2223 R 2223 R 2223 R 2223 R 2224 R 2223 R 3157 R	PART CODE RHEO876 RHEO912 RHEO372 RHEO372 RHEO372 RHEO372 RHEO372 RHEO372 RHEO372 RHEO372 RHEO372 RHEO376 RHEO376 RHEO376 RHEO364 RHEO376 RHEO352 RHEO358 RHE0	R.HETAL R.HETAL	F-782 SWP LOGIC R : Not used DESCRIPTION .0 KOHH +-53 1/8W .0 KOHH +-53 1/8W 470 OHH +-53 1/8W 30 OHH +-53 1/8W 31 OHH +-53 1/8W 1.0 KOHH +-53 1/8W 1.8 KOHH +-53 1/8W 1.7 KOHH +-13 1/4W 1.37KOHH13 1/4W 1/8W 10 OHH +-53 1/8W 10 OHH +-53 1/8W 10 OHH +-53 1/8W 100 OHH +-53 1/8W 100 OHH +-53 1/8W 10	
R 832 R 834 R 834 R 834 R 834 R 842 R 844 R 853 R 846 R 846 R 846	RHE00876 RHE00876 RHE0083 RHE0084 RHE00844 RHE00844 RHE00844 RHE008460 RHE008460 RHE00846 RHE00846 RHE00846 RHE00873 RHE100873 RHE100873 RHE100873 RHE008802 RHE008802 RHE008802	R.HETAL R.HETAL	1/34 1.0 K0HH +-52 1/34 1.0 K0HH +-52 1/34 3.9 K0HM +-52 1/34 47 K0HM +-52 1/34 100 0HH +-52 1/34 100 0HH +-52 1/34 100 0HH +-52 1/34 47 0HH52 1/34 47 K0HH +-52 1/34 47 K0HH +-52 1/34 47 K0HH +-52 1/34 47 K0HH +-52 1/34 3.32K0HH12 1/34 540 0HH +-52 1/34 2.2 K0HH +-52 1/34 2.2 K0HH +-53 1/34 3.2 X0H +-53	1 1 R R 1 1 1 1 1 1 1 1 1 1 1 1	R 22230 R 2230 R 2231 R 22354 R 22354 R 22354 R 22354 R 22454 R 22354 R 22454 R 22454 R 22454 R 22454 R 22454 R 22454 R 22454 R 2354 R 2354 R 2354 R 22456 R 2354 R 2354 R 2354 R 23554 R 2354 R 23557 R 23557 R 23557 R 23557 R 23557 R 23557 R 35557 R 35577 R 35577 R 355777 R 35577777777777777777777777777777777777	R ME 1088 RME 0852 RME 0852 RE 0766 RC 0766 RC 0766 RME 0766 RME 0384 RME 1155 RME 1711 RC 0757 RME 0846 RME 0864 RME 0864 RME 0864 RME 0864	R.METAL R.METAL R.METAL R.CARBONN R.CARBONN R.CARBONN R.METAL R.METAL R.METAL R.METAL R.CARBON R.CARBON R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	
R 867 R 872 R 872 R 874 R 874 R 874 R 874 R 881 R 883 R 883 R 885 R 885 R 885 R 885 R 810	RME0876 RME0879 RME0864 RME0864 RME0885 RME0885 RME1070 RME0876 RME1070 RME0876 RME0876 RME0881 RME0884 RME0864 RME0875	R,METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL R.METAL	1/84 1.0 KOHH +-52 1/84 1.0 KOHH +-52 1/84 100 00HH +-52 1/84 100 00HH +-52 1/84 1.0 KOHH +-52 1/84 5.6 KOHH +-52 1/84 5.6 KOHH +-52 1/84 681 0HH +-12 1/84 0.0 KOHH +-52 1/84 100 0HH +-52 1/84 100 0HH +-52 1/84 820 0HH +-52	1 1 1 1 R R 1 1 1 1 1 1 1 1 1 1	RH 2211 RH 2232 RT 847 RV 675 RV 675 RV 801 RV 801 RV 814 RV 814 RV 876 RV 884	ACE0852 RCE0852 RCE0854 HDD0086 RNE0047 RNE0047 RNE0047 RNE0042 RNE0042 RNE0042 RNE0042 RNE0070			

A. 1 (V-2023) P. 1 (V-2024) P. 1 (V-

PANEL (PEF-783) POWER (PEF-784) A : VC-6025 B : VC-6045 PEF-784 POWER SUPPLY . vc-6025 B : VC-6045 PEF-783 PANEL 0.T B 1 DESCRIPTION SHEET 35%55 UL54V-1 SHEET 25%25 UL94V-1 SHEET 25%15 UL94V-1 8. TY 1 ..PART CODE.. 8480992 8480993 .. PART CODE.. Hylood2 SYMBOL CCG0211 CCG0211 CCG0211 CCG0211 C.CERAMIC C.CERAMIC C.CERAMIC C.CERAMIC 1601 1602 1604 1605 50 V10000 50 V10000 50 V10000 50 V10000 PF+-10% PF+-10% PF+-10% PF+-10% 84884993 1 1 1 1 1 1 1 0000 CAPACITOR C.PLASTIC C.CERANIC CCC1030 CCC1002 CCC1002 CCC1002 CCC10027 CCC10027 CCC10027 CCC1007 CCC107 CCC107 CCC107 CCC1027 CCC107 CCC1027 CCC107 CCC007 CCC 1 8855678892312345614887999100011100 1 1 1 1 HDP0033 8392133 8392133 8392133 8392133 8392133 8392133 8392133 8392133 0100E(LEO) 0100E 0100E D10DE 0100E 0100E 0100E 0100E D10DE D100E 50 V10 P65534SY GL-9PR2 GL-9PR2 GL-9PR2 GL-9PR2 GL-9PR2 GL-9PR2 GL-9PR2 GL-9PR2 1601 1602 1605 1606 1607 1608 1609 1610 1611 0000 1 111 444444444444 111111 1 1 1 1 1 1 1 0000 ő 10H1258 IDH1258 1C.DIGITAL 1 1 IC 1601 H074LS164P/SN74LS164N HD74LS164P/SN74LS164N HD74L5164P/S 1/84 540 1/84 540 1/84 540 1/84 540 1/84 540 1/84 540 1/84 540 1/84 540 1/84 540 1/84 540 1/84 100 1/84 220 1/84 100 1/84 100 1/84 100 1/84 100 1/84 00 RME0873 RME0873 RME0873 RME0873 RME0873 RME0873 RME0873 RME08844 RME08844 RME08844 RME08844 RME08844 RME08844 RME08844 RME089928 RME10609 RME110609 RME110609 RME11054 R.METAL 1111 į 1011 1013 1020 1021 1022 1023 1024 1031 1033 1034 1035 1044 1043 10443 1045 1045 1045 1 1 1 1 1111 1 1 1 1 1 1 1 1111 EXB-LE5 5028(581T.5K) EXB-LE5 5028(581T.5K) EXB-LE5 5028(581T.5K) RZA0202 RZA0202 RZA0202 R.BLOCK R.BLOCK R.BLOCK RM 1601 RM 1602 RM 1603 111 1 1111111111 RDV0546 RNR0209 RDV0545 RDV0546 RDV0546 RNR0210 R0V0546 RNR0229 VR.CARBON VR.METAL VR.CARBON VR.CARBON VR.CARBON VR.METAL VR.CARBON VR METAL $\begin{array}{cccc} v_{12L5}(PVB) + n10 kOHM & SHAFT16\\ 1/2 & 10 kOHM8 & + 25 x\\ v_{12L5}(PVB) + 1 KOHM & SHAFT16\\ v_{12L5}(PVB) + 110 kOHM & SHAFT16\\ v_{12L5}(PVB) + 110 kOHM & SHAFT18\\ v_{12L5}(PVB) + 10 kOHM & - 25 x\\ v_{12L5}(PVB) + 10 kOHM & - 25 x\\ v_{12L5}(PVB) + 10 kOHM & L35\\ \end{array}$ RV 1601 RV 1602 RV 1603 RV 1603 RV 1605 RV 1605 RV 1606 RV 1607 RV 2400 1 1 1 1 1 1256 1257 1258 1259 1280 1281 1282 1502 1503 504 111 111 SW. PUSH SPPH2 TYPE-A NONLOCK 1 CC00338 C.CERAMIC C.CERAMIC S 1601 \$\$P0572 1 5 PEF-784 PDWER SUPPLY C.CERAMIC DET100F22M-VA1-KC C.AL ELYC 400 V SO V54 UF +-20X C.AL ELYC 50 V C.AL ELYC 25 V C.AL ELYC 25 V C.AL ELYC 16 V C.AL ELYC 160 V C.AL ELYC 164 NODOC C.AL ELYC 164 NODOC C.AL ELYC 164 NODUF +-20X C.AL ELYC 164 NOUF +-20X C.AL ELYC A : VC-6025 A : VC-6025 B : VC-6045 B : VC-6045 PEF-784 POWER SUPPLY PEF-783 PANEL 8.T B 1 1 PEF-FOS PAREL SW.LEVER ALSS-274 (WITH NOB AZ4004) SW.PUSH SPH1 TYPE-A SELFLOCK SU.PUSH SPUSUS (STROKEL, SMR.RESET) SU.PUSH SPUSUE (STROKEL, SMR.RESET) .. PART CODE... S\$L0076 S\$P0570 S\$P0573 S\$P0571 S\$P0573 S\$P0571 S\$P0570 *50570 8.TY SYMBOL \$ 1603 \$ 1605 \$ 1606 \$ 1607 \$ 1608 \$ 1609 \$ 1610 \$ 1611 \$ 1612 SYMBOL B111111111 111111111 SSP0570 SSP0570 1 1 1 TZ032050NR169 (~5P) 1 C.VARIABLE 1 CVT0054 c٧ 859 HDM0139 HDM0139 HDS0437 HDS0437 HDM0051 HDM0051 HDM0051 HDX0055 HDS0437 MTZ 3.3JA MTZ 3.3JA 15513 145143 145143 155165 MA164 155165 155135 155133 MTZ 3.3JA MTZ 12JC 155133 155133 155133 155133 155133 155133 155133 155133 155133 155133 D100E 1111 1 D 862 863 871 872 873 873 874 874 874 874 874 874 874 902 903 i 1 1 HD\$0437 910 911 1013 1022 1023 1024 1026 1029 1030 1031 1032 1040 1041 000000 1 H0 5 0 2 5 0 HD 5 0 2 5 0 15583

A : VC-602	3 : VC-6045	PEF-	784 POWER SUPPLY		A : VC-602	3 ; VC-6045	Р	EF-784 POWER SUPPLY	
SYMBOL	PART CODE		ESCRIPTION	A B	SYMBOL	PART CODE		. DESCRIPTION	····· 4.17].
0 1042	H050250	30010	15583		R 1019 R 1020	RCE0755 RCE0779	R.CARBON R.CARBON	1/4W 68 OHM +-5% 1/4W 6.8 KOHM +-5%	1 1
0 1043	H0S0250 H0M0141	0100E 0100E	18883 MT2 7.5JC		R 1021	RCE0750	R.CARBON	1/4W 8.2 KOHM +-52	1 1 1
0 1280	H0M0141	0100E	MTZ 7.5JC	i	R 1022	RCE0787	R.CARBON	1/4W 33 KOHM +-5x	i i
0 1281	H0S0250	DIOOE	15583		R 1023 R 1024	RME1261 RME1726	R.METAL R.METAL	1/4W 43.2 K OHM +-1x	1 1
0 1282	H0\$0250 HD\$0250	0100E 0100E	1 \$ \$ 8 3 1 \$ \$ 8 3		R 1025	RCE0779	R.CARBON	ERO-S2CKF2432(24.3K)/SN14 1/4W 6.8 KOHM +-5X	1 1 1
0 1284	H0\$0250	0100E	15583	i	R 1026	RCE0775	R.CARBON	1/4W 3.3 KOHM +-5X	i i
0 1501 D 1502	H0R0234 H0G0082	0100E	RBV-406		R 1027 R 1028	RCE0763 RME1759	R, CARBON R.METAL	1/4W 330 OHM +-5% 2W 3.3 KOHM +-5%	1 1
0 1503	H040071	0100E 0100E	GZB 3.08 Aug1		R 1029	RCE0785	R.CARBON	1/4W 22 KOHM +-5%	
0 1504	HDA0071	0100E	AU01	1 1 1	R 1032	RCE0715	R.CARBON	1/2W 6.8 KOHM +-5%	i i
D 1514 0 1515	H0G0081 H0G0083	0100E 010DE	GZB 2.48 GZB 6.88		R 1035 R 1040	RMV0012 RCE0798	R.METAL R.CARBON	VR37 15 MOHM +-1% 1/4W 330 Kohm +-5%	1 1 1
0 1520	HDD0141	OIODE	DTAIDE	i	R 1041	RCE0769	R.CARBON	1/4W 1.0 KOHM +-5%	1 1
0 1521	H0A0071	DIOOE	AU01		R 1042 R 1043	RCE0790 RSE0434	R . CARBON	1/4W 56 KOHM +-5X 1/4W 10 MOHM +-5X	1 1
0 1531	HDA0074 H0A0071	DIOOE	AU01A AU01		R 1251	RCE0795	R.SOLIO R.CARBON	1/4W 150 KOHM +-5%	
D 1551	HDF0053	OIOOE	FM8-26		R 1252	RMV0012	R.METAL	VR37 15 MOHM +-1%	i i
0 1561	HDF0052 H0F0053	0100E 0100E	FMB-24		R 1253 R 1254	RSE0434 RMV0014	R.SOLIO R.METAL	1/4W 10 MOHM +-5% 1/2W 6.20 M#-4 +-1.0%	1 1
0 1591	H050437	0100E	FMB-26 155133		R 1255	RCE0735	R.CARBON	1/2W 1.0 MOHN +-5%	
1					R 1256	RCE0792	R.CARBON	1/4W 82 KOHM +-5%	1 1
F 1001	EFZ0013	ICPROTECT	ICP-F10 (0.4A)	1 1	R 1257 R 1258	RCE0794 RCE0781	R-CARBON R-CARBON	1/4W 120 KOHM +-5X 1/4W 10 KOHM +-5X	1 1
IC 1501	1250109	IC.HYBRIO	STK7308	1 1	R 1259	RCE0717	R.CARBON	1/2W 10.0 KOHM +-5%	i i [
IC 1591	HZP0030	PHOTOCOPUL	PC714V	1 1	R 1260 R 1271	RCE0725 RCE0781	R . CARBON	1/2W 47 KOHM +-5%	1 1
J 1502	ETZ0121	TAB	62747-1		R 1272	RCE0794	R.CARBON R.CARBON	1/4W 10 KOHM +-5X 1/4W 120 KOHM +-5X	1 11
J 1503	ETZ0121	TAB	62747-1		R 1280	RCE0786	R.CARBON	1/4W 27 KOHM +-5x	i i
					R 1281 R 1282	RCE0781 RCE0785	R.CARBON R.CARBON	1/4W 10 KOHM +-5% 1/4W 22 KOHM +-5%	1 1 1
L 1001	TLE0173 TLE0172	COIL	EL0607SKI 101K (100UH) EL0607SKI 470K (47UH)		R 1283	RCE0757	R.CARBON	1/4W 22 KUHM +-5X	
L 1502	TLL0174	COIL	LC0243	1 1 i	R 1284	RCE0757	R.CARBON	1/4W 100 OHM +-5%	1 1
L 1510	TLX0175	COIL	BLOZRN1-R62		R 1501 R 1502	RWK0003 RWK0002	R.WIRE R.WIRE	3W 10 0HM+-5X 3W 2 0HM+-5X	1 1 1
L 1511 L 1532	TLX0175 TLT0085	COIL	BL02RN1-R62 47 UH+-10X 0.94A		R 1503	RCE0729	R.CARBON	1/2W 100 KOHN +-5%	
L 1542	TLT0085	COIL	47 UH+-10% 0.94A	1 1 1	R 1504	RCE0729	R.CARBON	1/2W 100 KOHM +-5%	i i
L 1552 L 1562	TL T0086 TL T0086	COIL	22 UH+-10X 1.3 A 22 UH+-10X 1.3 A		R 1505 R 1506	RCE0769 RCE0783	R.CARBON R.CARBON	1/4W 1.0 KOHM +-5X 1/4W 15 KOHM +-5X	1 1
L 1572	TL T0086	COIL	22 UH+-102 1.3 A 22 UH+-102 1.3 A		R 1506	RCE0782	R.CARBON	1/4W 12 KOHM +-5%	1
					R 1507	RCE0778	R.CARBON	1/4W 5.6 KOHM +-5X	1 1
P 851 P 890	J880060 J880021	CONNECTOR	858-XH-A 838-XH-A		R 1508 R 1509	RCE0779 RCE0782	R.CARBON R.CARBON	1/4W 6.8 KOHM +-5%	1 1
P 1042	J880022	CONNECTOR	868-XH-A		R 1512	RMR2791	R.METAL	2 W 47 OHM +-5%	i i [
P 1280	J880021	CONNECTOR	838-XH-A		R 1515 R 1521	RCE0773 RCE0685	R.CARBON R.CARBON	1/4W 2.2 KOHM +-5% 1/2W 22 OHM +-5%	1 1 1
P 1290 P 1501	J880021 J880024	CONNECTOR	838-XH-A 8158-XH-A		R 1521 R 1522	RMR2789	R.METAL	1/2W 22 0HM +-5X 2 W 22 0HM +-5X	
P 1502	JBB0023	CONNECTOR	888-XH-A	i i i	R 1591	RCE0729	R.CARBON	1/2W 100 KOHM +-5%	i i
R 850	RCE0903	R.CARBON	1/4W 1.5 MOHM +-5X		R 1592 R 1593	RCE0729 RCE0789	R.CARBON R.CARBON	1/2W 100 KOHM +-5X 1/4W 47 KOHM +-5X	1 1
R 850	RSE0434	R.SOLIO	1/4W 1.5 MOHM +-5%		1 1 373	ACCUIDY	R.CARBON	1/4W 4/ KUNN +-5X	1 1
R 851	RCE0756	R.CARBON	1/4W 82 OHM +-5%		RV 1042	RNEOO88	VR.METAL	EVM-K3GA00854(50K)	1 1
R 852 R 855	RCE0756 RCE0775	R,CARBON R,CARBON	1/4W 82 OHM +-5% 1/4W 3.3 KOHM +-5%		RV 1253 RV 1281	RNE0089 RNE0089	VR.METAL VR.METAL	EVM-K3GA00B15(100K) EVM-K3GA00B15(100K)	
R 855	RCE0780	R.CARBON	1/4W 8.2 KOHM +-5%		RV 1506	RNE0087	VR.METAL	EVM-K3GAOOB53(5K)	i i
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				1	1				
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V OUT (PEF-785)

	785 V-0UT		A : VC-6025	B : VC-6045	PFF-	785 V-OUT	
A: VC-6025 B: V SYMBOL	$\begin{array}{c} \hline \hline $ 285 \ V-001 \\ \hline $ 850 \ V-001 \\ \hline $ 12-5C \\ \hline $ 14 \ V \ 47 \\ \hline $ 12-5C \\ \hline $ 14 \ V \ 47 \\ \hline $ 16 \ V \ 1000 \\ \hline $ 16 \ V \ 10000 \\ \hline $ 16 \ V \ 1000 \\ \hline $ 16 \ V \ 10000 \\ \hline $ 16 \ V \ 1000 \\ \hline $ 10 \ V \ 1000 \ V \ 1000 \\ \hline $ 10 \ V \ 1000 \ V \ 10000 \ V \ 1000 \ V \ 10000 \ V \ 10000$	O. IY A B 1 1 <tr< th=""><th>A : VC-6025 SYMBOL R 537 R 537 R 537 R 544 R 555 R 556 R 555 R 557 R 557 R 577 R 577 R</th><th>D : VC-6045PART CODE RHE0862 RHE0862 RHE0858 RHE0858 RHE1051 RHE1051 RHE1051 RHE1051 RHE1051 RHE1051 RHE1051 RHE1051 RHE1061 RHE1063 RHE1063 RHE1063 RHE1063 RHE1063 RHE1064 RHE1064 RHE1064 RHE1065 RHE1065 RHE1065 RHE1064 RHE1064 RHE1065 RHE1065 RHE1064 RHE1064 RHE1064 RHE1065 RHE1065 RHE1064 RHE1064 RHE1064 RHE1064 RHE1065 RHE00857 RHE00857 RHE00857 RHE02971 RHE02974 <</th><th></th><th>Z45 Y-OUT ESCRIPTION </th><th>C C . IY A B 1</th></tr<>	A : VC-6025 SYMBOL R 537 R 537 R 537 R 544 R 555 R 556 R 555 R 557 R 557 R 577 R	D : VC-6045PART CODE RHE0862 RHE0862 RHE0858 RHE0858 RHE1051 RHE1051 RHE1051 RHE1051 RHE1051 RHE1051 RHE1051 RHE1051 RHE1061 RHE1063 RHE1063 RHE1063 RHE1063 RHE1063 RHE1064 RHE1064 RHE1064 RHE1065 RHE1065 RHE1065 RHE1064 RHE1064 RHE1065 RHE1065 RHE1064 RHE1064 RHE1064 RHE1065 RHE1065 RHE1064 RHE1064 RHE1064 RHE1064 RHE1065 RHE00857 RHE00857 RHE00857 RHE02971 RHE02974 <		Z45 Y-OUT ESCRIPTION	C C . IY A B 1
A : VC-6025 B : SYMBOL IC 1301 I DH0339 JP 1 RHE0912 L 563 8376796 L 564 8376796 L 564 8376796 L 564 8376796 L 564 8376796 L 564 8376796 L 564 8376796 R 502 JB80027 P 502 JB80027 P 503 883570 R 501 RC1040 R 503 RH10400 R 508 RH10400 R 508 RH10400 R 508 RH10866 R 512 RH10866 R 513 RH10866 R 513 RH10866 R 513 RH10866 R 514 RC10715 R 515 RH10866 R 515 RH108673 R 517 RH10866 R 512 RH108673 R 517 RH108673 R 517 RH108673 R 517 RH108673 R 518 RH108673 R 517 RH10873 R 517 RH108673 R 517 RH10873	2785 V-OUT R : Not Used MM3102 NAM 1/8W 0 O NHM T-COIL(3T,TT) TCOIL(3T,TT) TCOIL(3T,TT) TCOIL(3T,TT) TAW 500 OMH -512 TAW TAW 100 OMH -512 TAW 120 OMH -512 TAW 150 OMH -512 TAW 150 OMH -512 TAW 150 OMH -512 <th></th> <th>A : VC-602 SYMBOL R 552 R 591 R 592 R 593 R 593 R 1302 R 1302 R 1303 RV 574 RV 1503 TR 501 TR 503 TR 503 TR 541 TR 542A TR 544A TR 544A T</th> <th>5 B : VC-604 . PART CODE RHE 0340 RHE 0340 RHE 0340 RHE 0340 RHE 0340 RHE 1045 RHE 1045 RHE 1045 RHE 045 RHE 045</th> <th></th> <th>-785 V-DUT DESCR PTION</th> <th></th>		A : VC-602 SYMBOL R 552 R 591 R 592 R 593 R 593 R 1302 R 1302 R 1303 RV 574 RV 1503 TR 501 TR 503 TR 503 TR 541 TR 542A TR 544A TR 544A T	5 B : VC-604 . PART CODE RHE 0340 RHE 0340 RHE 0340 RHE 0340 RHE 0340 RHE 1045 RHE 1045 RHE 1045 RHE 045 RHE 045		-785 V-DUT DESCR PTION	

CRT SOCKET 1 (PEF-789)

CRT SOCKET 2 (PEF-835)

		(/	
A : VC-602	5 B: VC-604	JEI LOY CHI SOCALI	
SYMBOL C 1044 C 1045	PART CODE CCD0231 CCC1025	C.CERAMIC 2000 V 4700 PF+80-20X C.CERAMIC 2000 V 4700 PF+80-20X C.CERAMIC S0 V 100 PF+-10X	Q.TY A B 1 1
J 1001	8390152	SOCKET 1339	1
L 1061 L 1062	TLE0107 TLE0107	INDUCTOR ELE-Y R47 MA Inductor ELE-y R47 Ma	1
NL 1043	EL\$0032	LAMP SA-200DSS-ON-1	1
P 1001 P 1043 P 1061 P 1062 P 1281	JBS0022 JB80022 ETP0002 ETP0002 JB80021	CONNECTOR SJ8-XH-A CONNECTOR B68-XH-A PIN 17/255-1 PIN 17/255-1 CONNECTOR B38-XH-A	1 1 1 1
R 1061 R 1062 R 1066 R 1067	RME1722 RME1722 RCE0781 RCE0745	R.METAL 1/4W 165 7-4+-1.0X R.METAL 1/4W 165 7-4+-1.0X R.CARBON 1/4W 10 60HH +-5X R.CARBON 1/4W 10 60HH +-5X	1
L	L	1	
FILTER	(PEF-81	•	
SYMBOL	PART CODE		···· 0.1Y
C 1501 C 1510	CQE0118 CQE0118	C PLASTIC ECQ-E2A224MW C PLASTIC ECQ-E2A224MW C PLASTIC ECQ-E2A224MW	A B 1 1 1 1
L 1501	TLP0043	COIL 250VAC 15MH	1 1
R 1510	RCE0733	R.CARBON 1/2W 470 KOHM +-5%	1 1
SG 1501 SG 1502	EZH0084 EZH0084	AG20 P C 252F-L3N AG20 P C 252F-L3N	1 1

ATT READOUT (PEF-833)

	5 B : VC-604	5 PEF-833 ATT READOUT	
SYMBOL RM 5153(PART CODE RZA0202	R.BLOCK EXB-LES SO2S(SBIT.SK)	9.TY A B 1 1

A : VC-6025 B	: VC-6C45 PE	F-835 CRT SOCKET2	
	T CODE		· · · · · · · · · · · · · · · · · · ·
C 1055 CCC10		50 V 100 PF+-102	
J 1011 83901	SZ SOCKET	1339	1
L 1071 TLE01	09 INOUCTOR	ELE-Y R68 MA	1
L 1072 TLE01	09 INDUCTOR	ELE-Y R68 MA	1
NL 1053 ELSOO		SA-200035-0N-1	1
P 1011 JBS00 P 1053 JB800 P 1071 ETP00 P 1072 ETP00 P 1291 JB800	22 CONNECTOR 02 PIN 02 PIN	S3B-XH-A B6B-XH-A 171255-1 171255-1 B3B-XH-A	
R 1071 RME10 R 1071 RME10 R 1072 RME10 R 1072 RME10 R 1076 RCE07 R 1077 RCE07	68 R.METAL 62 R.METAL 68 R.METAL 81 R.CARBON	1/4W 150 OHM +-1x 1/4W 475 OHM +-1x 1/4W 150 OHM +-1x 1/4W 475 OHM +-1x 1/4W 475 OHM +-5x 1/4W 10 KOHM +-5x	1 1 1 1
		*	
			J

CYCLE (PEF-837)

A : VC-602	5 B : VC-604	S PEF	-837 CYCLE	
SYMBOL	PART CODE		DESCRIPTION	A B
C 2003	CES0033	C.AL ELYC	25 V 100 UF+-20%	1 7 7
C 2005	CQA0121	C.PLASTIC	50 V33000 PF+-10x	1 i i
C 2006	C0A0122	C.PLASTIC	50 V47000 PF+-10X	1 i i
C 2007	CE\$0378	C.AL ELYC	16 V 330 UF +-20%	1 1 1
C 2008	CE\$0378	C.AL ELYC	16 V 330 UF +-20X	1 1 1
C 2012	CMD0947	C.MICA	300 V 470 PF+-5%	1 1
C 2013	CQE0116	C.PLASTIC	100 V 0.47UF+-5%	1 1 1
C 2014	CCG0211	C.CERAMIC	50 V10000 PF+-10%	1 1
C 2015 C 2016	CCG0213 CCG0211	C.CERAMIC	50 V 0.1 UF+80-20%	1 1
C 2017	CQA0132	C.CERAMIC	50 V10000 PF+-10x	1 1
C 2038	CQA0132	C.PLASTIC C.PLASTIC	50 V 0.33UF+-10X 50 V 0.33UF+-10X	1 1
C 2039	CC60213	C.CERAMIC	50 V 0.33UF+-10X 50 V 0.1 UF+80-20X	
C 2042	CC60207	C.CERAMIC	50 V 2200 PF+-10X	
C 2043	CE\$0038	C.AL ELYC	50 V 2.2 UF+-20%	
C 2050	CCG0211	C.CERAMIC	50 V10000 PF+-10%	1 i i
C 2051	CCG0211	C.CERAMIC	50 V10000 PF+-10X	li i
C 2052	CCG0211	C.CERAMIC	50 V10000 PF+-10X	1 i i
C 2060	CCG0136	C.CERAMIC	50 V 33 PF+-5%	1 i i
C 2061	CCG0211	C.CERAMIC	50 V10000 PF+-10x	1 i i
C 2070	CE\$0133	C.AL ELYC	16 V 47 UF+-20x	1 1
C 2071	CESC133	C.AL ELYC	16 V 47 UF+-20X	1 1
C 2072	CE\$0133	C.AL ELYC	16 V 47 UF+-20%	1 1
C 2092	CCG0144	C.CERAMIC	50 V 220 PF+-5x	1 1
D 2004 D 2020	HDS0437 HDM0139	DIODE	1\$\$133	1 1 1
		DIODE	MTZ 3.3JA	1 1
IC 2040	ILT0045	IC.ANALOG	TL064CN	1 1 1
IC 2050	ILN0085	IC.ANALOG	NJM 3190	1 1
IC 2052	1001221	IC.DIGITAL	HO74LSOOP/SN74LSOON	1 1
IC 2090	HT00161	TRANSISTOR	OTC124EK	1 1 1
IC 2091	HT00161	TRANSISTOR	DTC124EK	1 1
L 2092	TLE0072	COIL	EL06065KI 220 UH+-10%	1 1
P 2001 P 2002	JB\$0071 JB\$0027	CONNECTOR	SQ-10-AP-GB-C SQ-8-AP-GB-C	1 1
R 2001	RME0384	R.METAL	1/8W 4.7 KOHM +-5X	1 1 1
R 2002	RME0902	R.METAL	1/8W 220 KOHM +-5X	
R 2003	RME0869	R.METAL	1/8W 270 OHM +-5X	1 1 1
R 2004	RME0884	R.METAL	1/84 4.7 KOHM +-5%	li i
R 2005	RME0907	R.METAL	1/8W 2.2 MOHM +-10X	1 1 1
R 2006	RME0907	R.METAL	1/8W 2.2 MOHM +-10X	1 1
R 2007	RME1064	R.METAL	1/4W 221 OHM +-1X	1 1
R 2010	RME0850	R.METAL	1/8W 2.2 KOHM +-5%	1 1 1
R 2011 R 2012	RME0882 RME0896	R.METAL	1/8W 3.3 KOHM +-5x	1 1
R 2012 R 2013	RME0896	R.METAL R.METAL	1/8W 47 KOHM +-5X	1 1
R 2015	RME0892	R.METAL	1/8W 2.2 KOHM +-5% 1/8W 22 KOHM +-5%	1 1
R 2015	RME0896	R.METAL	1/8W 22 KOHM +-5X 1/8W 47 Kohm +-5X	
R 2017	RME0912	R.METAL	1/8W 0 0HM	1 1
R 2020	RCE0716	R.CARBON	1/2W 8.2 KOHM +-5x	
R 2021	R/151714	R.METAL	1/4W 221 KOHM +-0.5x	
R 2022	RME1713	R.METAL	1/4W 22.1 KOHM +-0.5%	1 1
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6.17 1 1 1 1 1 1]	0.1Y B 1 3 5 1 1 1 1 1 1 1 1	********************************	
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CZ121 GSI42R3 BNC071 1/4W 1/4W	F-880 DIGIT	DESCRIPTIO IC61-03 DP-10 50 50 50 50 50 16 50 50 50 50 50 50 50 50 50 50 50 50 50	14 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
		SOCKET.IC PIN C.CERAMIC C.CERAMIC C.CERAMIC C.CERAMIC C.CERAMIC C.CERAMIC C.CERAMIC C.CERAMIC C.CERAMIC	C.AL ELYC C.CER ANIC C.CER ALLYC C.CER ANIC C.CERANIC	×
B : VC-604 PART CODE 2474249 JS60002 JH80088 RCE0745 RCE0745 RCE0756 DPX0090 DPX0091	L (PEF-8	PART CODE IV10101 ETP0149 CC60292 CC60292 CC60292 CC60295 CC80295 CC80295 CC80295 CC80295 CC802146 CC602746 CC602746 CC602746 CC60292	$\begin{array}{c} C \le 0.1 \ 33 \\ C \le 0.1 \ 32 \\ C \le 0.2 \ 92 \\ C \le 0.1 \ 33 \\ C \le 0.2 \ 92 \\ C \le 0.1 \ 33 \\ C \le 0.2 \ 92 \\$	
A : VC-602 SVMB0L J 507 J 1501 R 101 R 101 V 1001 V 1001		SYHBOL C5300-12 C5314-16 C5320-24 C 5203 C 5204 C 5210 C 5254 C 5254 C 5260 C 5343 C 5344	C 5345 C 5346 C 53449 C 53349 C 53351 C 54001 C 54001 C 54002 C 55002 C 55002	
0. TY 5 1 1 1 1 1 1 1 1 1 1 1 1 1		0.17Y B 1 1 3 1 1 1 1	1 R 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
			1 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
BJ7 CYCLE BS CD PT ION	IS R + Not vord	L3 R Not used ESCRIPTION	3211475-BA 3211475-CB 3211475-CB 3211475-CB 3211475-CB 3211475-FA 321147	
	CHASS		CABLE . A SSY CABLE . A SSY CA	176
B : VC-6045 			3211484 A 3211475 CB 3211475 CB 3211475 CB 3211475 FA 3211475 FA 3	-
A : YC-602 SYMB 0L R 2023 R 2025 R 2026 R 2026 R 2050 R 2050 R 2057 R		SYMBOL	C 10 C 110 C 303 DL 490 F 1501 J 101 J 101 J 302	

A : VC-6025 B : VC-	045 PEF-880 DIGITAL		A : VC-6025 3 :	VC-6043	PEF-880 DIGITAL R : Not used								
SYMBOL PART COD C S524 CC60255 C S525 CC60283 C S526 CC60283 C S527 CC60283 C S528 CC60283 C S524 CC60283 C S5350 CC60282 C S545 CC60282 C S546 CC60282 C S547 CC60282 C S001 CC60282 C S002 C60283 C S003 CC60283 C S004 C604647 D S211 H010027 D S102. H0100447 D S102. H010027 D S102. H0100285 D S102. H010027	DESCRIPTION DESCRIPTION C.CERAMIC 50 V 5 PF0.25PF C.CERAMIC 50 V 50 PF0.25PF C.CERAMIC 50 V 50 PF53 C.ALELVC 16 V 470 UF20X C.ALELVC 10 V 470 UF20X C.CERAMIC 50 V 0.01UF10X C.CERAMIC C.CERAMIC 50 V 0.01U	0.1V 0.1V 1 1 </td <td>SYHBOL PARTA R 5101 PARTA R 5101 RHF109, R 5102 PART09, R 5102 PART09, R 5103 RHF109, R 5104 RHF123, R 5105 RHF107, R 5107 RHF124, R 5110 RHF144, R 5110 RHF144, R 5111 RHF144, R 5111 RHF144, R 5116 RHF142, R 5117 RHF144, R 5118 RHF144, R</td> <td>6 R. METTALL 6 R. METTALL 8 R. METALL 8 R. METALL 8 R. METALL 9 R. METALL <tr <="" td=""><td></td><td></td></tr><tr><td>A: VC-6025 B: VC- SYMBOL </td><td>R : Not used</td><td>A B A B 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</td><td></td><td>1 R. METTALL 8 R. METTALL 8 R. METTALL 8 R. METTALL 8 R. METTALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 1 R. METALL</td><td>PEF-380 DIGITAL R : Not used 1 OESCRIPTION </td><td></td></tr></td>	SYHBOL PARTA R 5101 PARTA R 5101 RHF109, R 5102 PART09, R 5102 PART09, R 5103 RHF109, R 5104 RHF123, R 5105 RHF107, R 5107 RHF124, R 5110 RHF144, R 5110 RHF144, R 5111 RHF144, R 5111 RHF144, R 5116 RHF142, R 5117 RHF144, R 5118 RHF144, R	6 R. METTALL 6 R. METTALL 8 R. METALL 8 R. METALL 8 R. METALL 9 R. METALL <tr <="" td=""><td></td><td></td></tr> <tr><td>A: VC-6025 B: VC- SYMBOL </td><td>R : Not used</td><td>A B A B 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</td><td></td><td>1 R. METTALL 8 R. METTALL 8 R. METTALL 8 R. METTALL 8 R. METTALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 1 R. METALL</td><td>PEF-380 DIGITAL R : Not used 1 OESCRIPTION </td><td></td></tr>			A: VC-6025 B: VC- SYMBOL	R : Not used	A B A B 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1 R. METTALL 8 R. METTALL 8 R. METTALL 8 R. METTALL 8 R. METTALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 1 R. METALL	PEF-380 DIGITAL R : Not used 1 OESCRIPTION	
A: VC-6025 B: VC- SYMBOL	R : Not used	A B A B 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1 R. METTALL 8 R. METTALL 8 R. METTALL 8 R. METTALL 8 R. METTALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 0 R. R. METALL 1 R. METALL	PEF-380 DIGITAL R : Not used 1 OESCRIPTION								

A : VC-6025					S	/H (PE				
SYMBOL R 8141A R 8141B RH 5301 RH 5301 RV 5202 RV 5202 RV 5302 RV 5301 RV 5301	D : VC-604 PART CODE MHE1413 RTA0326 R2A0326 R140326 R140326 RHE0058 RHE0058 RHE0058 RHE0054 R		-800 DIGITAL DESCRIPTION 0.1W 0 OHM 0.1W 0 OHM EXX-F1922070 EXX-F1922070 EXX-F1922070 EVN 35C00VB13(1K) EVN 35C00VB13(1K) EVN 35C00VB13(1K) EVN 35C00VB13(1K) EVN 35C00VB13(1K) EVN 35C00VB13(1K) EVN 35C00VB140) INV3 25C2759-U23 0TC124EK EXO-3(20HHZ)	G. IY A B 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		<pre>X : VC-6025 SYHBOL C : 5207 S201 C : 5207 C : 5252 C : 5253 C : 5254 C : 5254 C : 5254 C : 5554 C : 5049 C : 8049 D : 8049 D</pre>	B : VC-6045 PART CODE CC60226 CC60227 CC60227 CC602275 CC60275		T-383 5/H DESCRIPTION 0 5 0 0 1000 PF102 5 0 V 1000 PF102 5 0 V 1000 PF102 5 0 V 1000 PF52 5 0 V 1000 PF52 2 5 V 0.1 UF-80-202 2 5 V 0.1 UF-80-202 5 0 V 120 PF53 5 0 V 120 PF53 5 0 V 120 PF53 5 0 V 100 PF0.5F 5 0 V 100 PF0.5F 5 0 V 100 PF0.5F 5 0 V 100 PF0.5F 5 0 V 10 PF0.5F 5 0 V 0.01UF102 5 0 V 10 PF5.5F 5 0 V 0.01UF102 5 0 V 0.01UF102 5 0 V 0.01UF102 5 0 V 0.01UF022 5 0 V 0.1 UF-80-202 5 0 V 0.1 UF-80-2	
PANEL	(DSO) (P	-	-882 PANEL(DSO)			A : VC-602	5 B:VC-604	5 р	EF-883 S/H R : Not used	
SYMBOL R 1601 R 1603 R 1605 R 1605 S 1605 S 1605 S 1605 S 1606	PART CODE PRE1435 RHE1435 RHE1435 RHE1435 RSP0611 SSP0611 SSP0611 SSP0611 SSP0611	R. HETTAL R. HETTAL R. HETTAL R. HETTAL R. HETAL R. HETAL S. H. PB S. H. PB	DESCRIPTION			SPR R R R R R R R R R R R R R R R R R R		R R R R R R R R R R R R R R R R R R R	0 65 CE 1 P 1 D H 20 0 0 + + + 5 x 0 1 W 20 7 0 + H + - 5 x 0 1 W 2.7 K 0 + H + - 5 x 0 + H + - 5 x 0 1 W 2.7 K 0 + H + - 5 x 0 + H + - 5 x 0 1 W 100 0 + H + - 5 x 0 1 W 100 0 + H + - 5 x 0 1 W 1 + 7 K 0 + H + - 5 x 0 1 W 2.7 K 0 + H + - 5 x 0 1 W 2.7 K 0 + H + - 5 x 0 1 W 2.7 K 0 + H + - 5 x 0 1 W 2.7 K 0 + H + - 5 x 0 1 W 100 0 + H + - 5 x 0 1 W 100 0 + H + - 5 x 0 1 W 100 0 + H + - 5 x 0 1 W 100 0 + H + - 5 x 0 1 W 100 0 + H + - 5 x 0 1 W 1.0 K 0 + H + - 5 x 0 + H + - 5 x 0 1 W 1.0 K 0 + H + - 5 x 0 + H + - 5 x 0 1 W 1.0 K 0 + H + - 5 x 0 + H + - 5 x 0 1 W 1.0 K 0 + H + - 5 x 0 + H + - 5 x 0 1 W 1.0 K 0 + H + - 5 x 0 + H + - 5 x 0 1 W 1.0 K 0 + H + - 5 x 0 + H + - 5 x 0	G. FY G. F 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

A: VC-6025 B: VC	n_2016	DLY4 (PEF-886)
A : VC-6025 3 : VC SYVBOL PART CC R 30809 RME1420 R 30991 RME1420 R 30991 RME1420 R 30901 RME1420 R 30903 RME1420 R 3093 RME1420 R 3093 RME1420 R 3094 RME1424 R 3094 RME1424 R 3095 RME1424 R 3096 RME1424 R 3101 RME1428 R 3101 RME1428 R 3103 RME1428 R 3103 RME1424 R 3103 RME1424 R 3106 RME1424 R 3107 RME1424 R 3111 RME1427 R 31112 RME1428 R 3112 RME1428 R 3113 RME1428 R 3113 RME1428 R 3113 RME1428 R 3113 RME1428 R 3113 RME1428 R 3114 RME1427 R 3117 RME1429 R 3117 RME1429 R 3118 RME1428 R 3118 RME1428 R 3118 RME1428 R 3118 RME1428 R 3119 RME1428 R 3117 RME1429 R 3119 RME1450 R 3119 RME1450 R 3119 RME1428 R 3122 RME1428 R 3123 RME1428 R 3123 RME1428 R 3120 RME1428 R 3121 RME1428 R 3121 RME1428 R 3122 RME1428 R 3122 RME1428 R 3133 RME1428 R 3137 RME1428 R 314 RME1428 R 3153 RME1428 R 3153 RME1428 R 3154 RME1428 R 3155 RME1428 R 3157 RME1428 R 3557 RME1428 R 3064 RME028 TR 3257 RME028 TR	R : Not used	SYMBOL PAAT CODE DESCRIPTION
A : VC-6025 B : VC	2-6045 PEF-883 S/H	RS-232C (PEF-887)
A : VC-6025 B : VC SYMBOLPART CO TR 8066 H1C0848 TR 8067 H1C0846 TR 8069 H1C0846 TR 8067 H1C0846 TR 8070 H1C0846 TR 8072 H1C0846 TR 8072 H1C0846 TR 8072 H1C0846 TR 8072 H1C0846 TR 8072 H1C0846 TR 8072 H1C0846 TR 8074 H1C0846 T	, cr - vay 3/8	

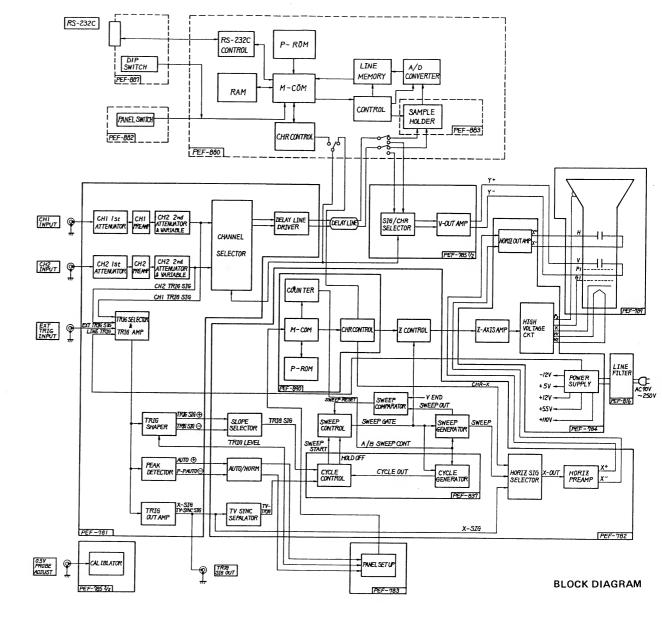
ROM PG CKT (PEF-890)

	5 B : VC-604	5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	E-890 ROM PG CKT	
SYMBOL	PART CODE IYT0003 IYX0041	SEAL (ROM) IC.SDCKET	DESCRIPTION 11X11MM T-TYPE MAT SILVER 10628-01-445	A B 1 1
C 3001 C 3002 C 3003 C 3005 C 3005 C 3005 C 3005 C 3007 C 3011 C 3012 C 3014 C 3014 C 3014 C 3014 C 3014 C 3014 C 3015 C 3016 C 3102 C 3105 C 3012 C 302 C 3	CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0211 CCG0205 CCG020	C.CERAMIC C.CERAMIC	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
D 3001 D 3002	HDM0139 HDS0437	DIODE DIODE	MTZ 3.3JA 158133	1 1
IC 3001 IC 3002 IC 3003 IC 3004 IC 3006 IC 3006 IC 3007 IC 3101 IC 3210 IC 3211 IC 3212	IDH1292 IDH1051 IOH1274 IDH1275 IDH1275 IDH1019 ILH0399 IDH0685 INH0017 IDH1149 IDH0982	IC.DIGITAL IC.DIGITAL IC.OIGITAL IC.DIGITAL IC.DIGITAL IC.DIGITAL IC.ANALOG IC.DIGITAL IC.DIGITAL IC.DIGITAL	HN27256G-25 HD74HC74P HD74HC74P HD74HC574P1C74HC573P HD74HC574P1C74HC574P HD74HC32P HN120D7HC32P HN120G-36 HH2264ALP-15 HD74HC155P HD74HC155P HD74HC00P/IC74HC00P	
P 3001 P 3002 P 3003 P 3004 P 3005 P 3006 P 3007 P 3008 P 3210	JBS0027 JBS0027 JBS0027 JBS0027 JBS0027 JBS0027 JBS0027 JBS0027 JBS0027 JBS0027 JBS0027 JBS0058	CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR CONNECTOR	S = -8 - AP - GB - C S = -AP - GB - C S = -A - AP - GB - C S = -8 - AP - GB - C B = 2B - KM - A	
R 3002	RME0892	R.METAL	1/8W 22 KOHN +-5x	1 1

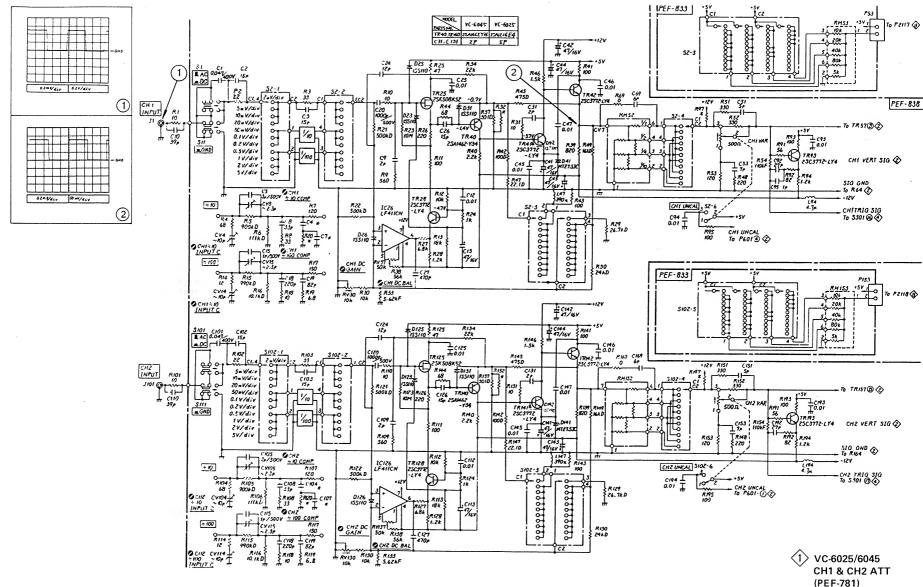
DLY5 (PEF-896)

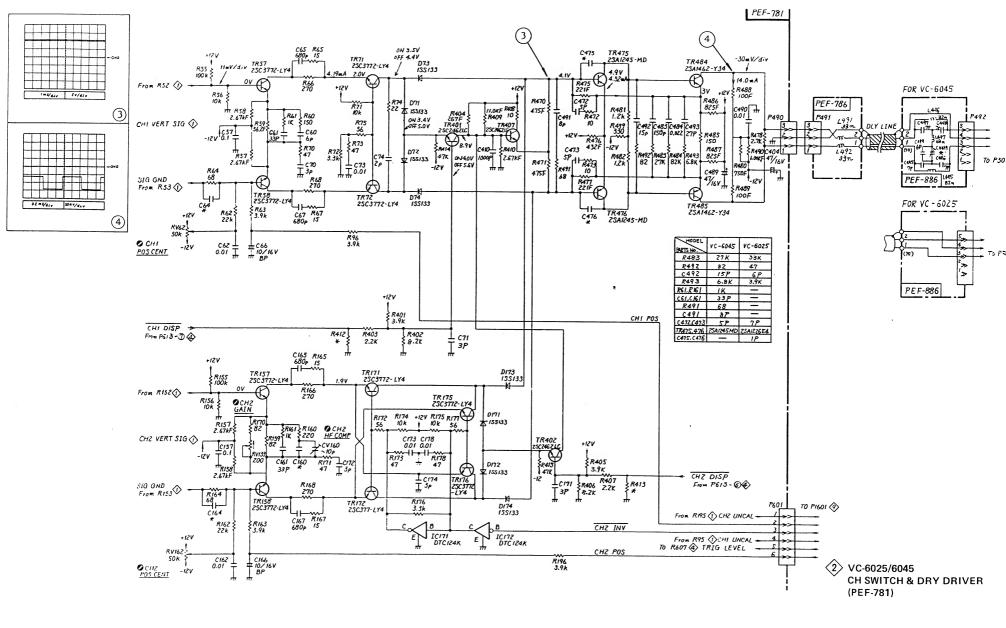
	A	: VC-602	•	5	PEF-896 DLY5					
	SYR L L	491 492	PART CODE TLN0015 TLN0015	COIL COIL	DESCRIPTION 0.033UH 0.033UH	4 5 0 MA 4 5 0 MA	+-20x +-20x	•••••	· · · · · · · · · · · · · · · · · · ·	9.TY B 1 1
	P	491	JBX2203	CONNECTOR	03JQ-ST				1	1
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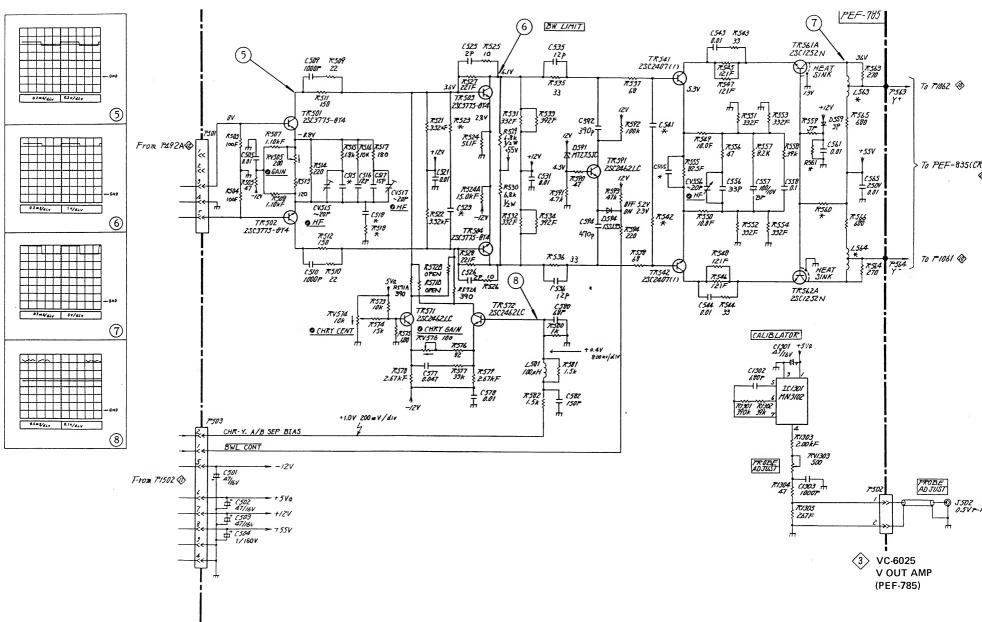
A : VC-602	5 B : VC-604	5 PER	-890 ROM PG CKT R : Not used
SYMBOL	PART CODE		DESCRIPTION B
R 3003	RME0892	R.METAL	1/8W 22 KOHM +-5% 1 1
R 3004	RME0892	R.METAL	1/8W 22 KOHM +-5% 1 1
R 3005	RME0884	R.METAL	1/8W 4.7 KOHM +-5% 1 1
R 3006 R 3010	RME0884	R.METAL	1/8W 4.7 KOHM +-5% 1 1
R 3010 R 3011	RMEC875 RME0875	ROMETAL	1/8W 820 OHM +-5X 1 1
R 3012	RME0375	R.METAL R.METAL	1/8W 820 0HM +-5X 1 1 1/8W 820 0HM +-5X 1 1
R 3013	RME0875	RIMETAL	1/8W 820 0HM +-5% 1 1 1/8W 820 0HM +-5% 1 1
R 3014	RMEO875	R.METAL	1/8W 820 OHM +-5% 1 1
R 3015	RMEOE75	R.METAL	1/8W 820 OHM +-5% 1 1
R 3016	RME0875	R.METAL	1/8W 820 0HM +-5% 1 1
R 3017	RMED875	R.METAL	1/8W 820 OHM +-5X 1 1
R 3018	RME0875	R.METAL	1/8W 820 OHM +-5x 1 1
R 3051 R 3052	RME0869	R.METAL	1/8W 270 OHM +-5x 1 1
R 3052 R 3053	RME0870 RME0880	R.METAL	1/8W 330 0HM +-5% 1 1 1/8W 2.2 KOHM +-5% 1 1
R 3054	RME0583	R.METAL R.METAL	1/8W 2.2 KOHM +-5% 1 1 1/8W 3.9 KOHM +-5% 1 1
R 3055	RME0862	R.METAL	1/8W 68 0HM +-5X 1 1
R 3056	RME0912	R.METAL	1/8W 0 0HM R R
R 3101	RILEOPOG	R.METAL	1/8W 1.0 MOHM +-5% 1 1
R 3210	RME0912	R.METAL	1/8W 0 0HM 1 1
R 3211	RME0912	R.METAL	1/8W O GHM IR R
R 3212	RME0912	R.METAL	1/8W 0 0HM 1 1
R 3213	RME0912	R.METAL	1/8W O CHM R R
R 3214	RME0912	R.METAL	1/8W 0 0HM 1 1
R 3215	RME0875	R.METAL	1/8W 820 OHM +-5x 1 1
R 3216	RMEC875	R.METAL	1/8W 820 OHM +-5x 1 1
R 3217 R 3218	RME0875	R.METAL	1/8W 820 OHH +-5% 1 1
R 3218 R 3219	RME0875	R.METAL R.METAL	1/8W 820 0HM +-5% 1 1 1/8W 820 0HM +-5% 1 1
R 3220	RME0875	RIMETAL	1/8W 820 0HM +-5X 1 1 1/8W 820 0HM +-5X 1 1
R 3221	RMEC875	R.METAL	1/8W 820 OHM +-5x 1 1
R 3251	RME0884	RIMETAL	1/8H 4.7 KOHM +-52 1 1
R 3252	RMEOSSS	R.METAL	1/8W 10 KOHM +-52 1 1
R 3253	RME0912	R. METAL	1/8W 0 0HM R R
R 3254	RME0864	R.METAL	1/8W 100 0HM +-5% 1 1
R 3257	RME0912	R.METAL	1/8W 0 0HM R R
R 3258	RME0912	R.METAL	1/5W 0 0HM 1 1
R 3556.	RME0896	R.METAL	1/8W 47 KOHM +-5X 2 2
TR 3001 TR 3002	HT40224 HTC0686	TRANSISTOR TRANSISTOR	25A1029 D 1 1 25C2462C 1 1
TR 3003	HTA0263	TRANSISTOR	25A1052D 1 1
TR 3201	HTC0590	TRANSISTOR	2SC162184 1 1
X 3101	AAH0089	XTAL	HC-49/U 12.000MHZ 1 1
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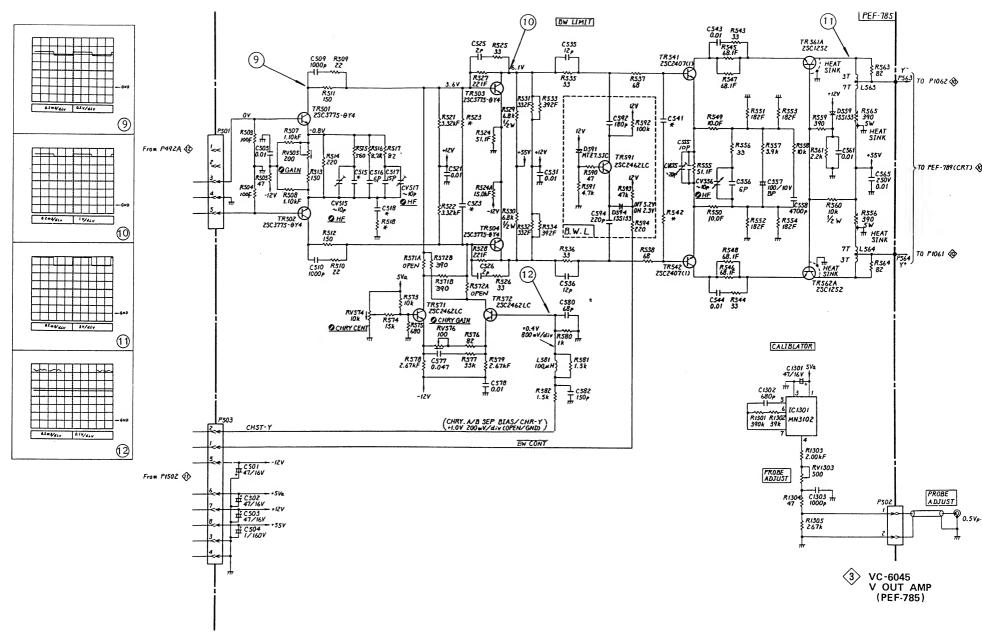


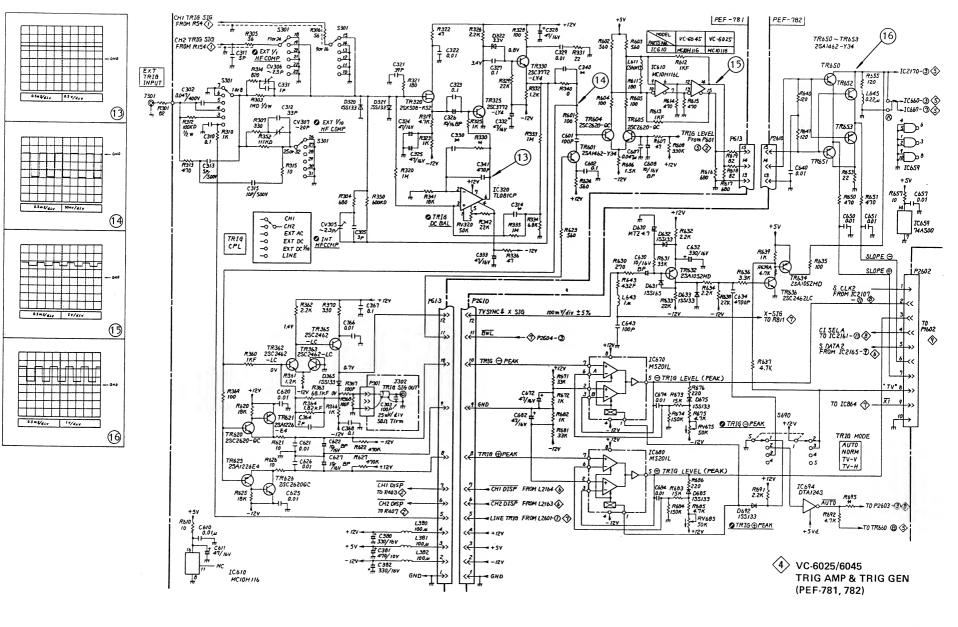
10. SCHEMATIC DIAGRAMS

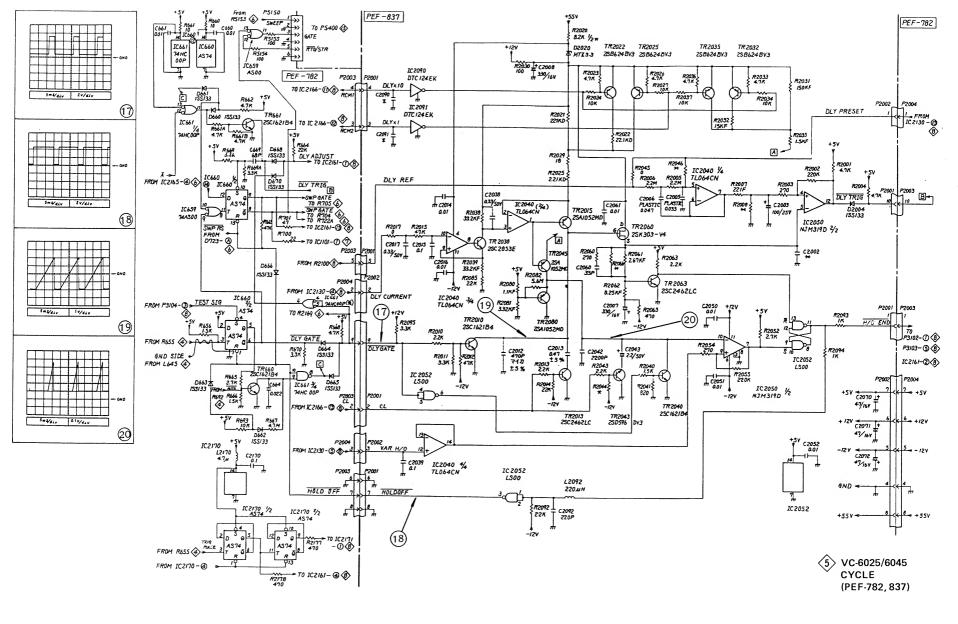


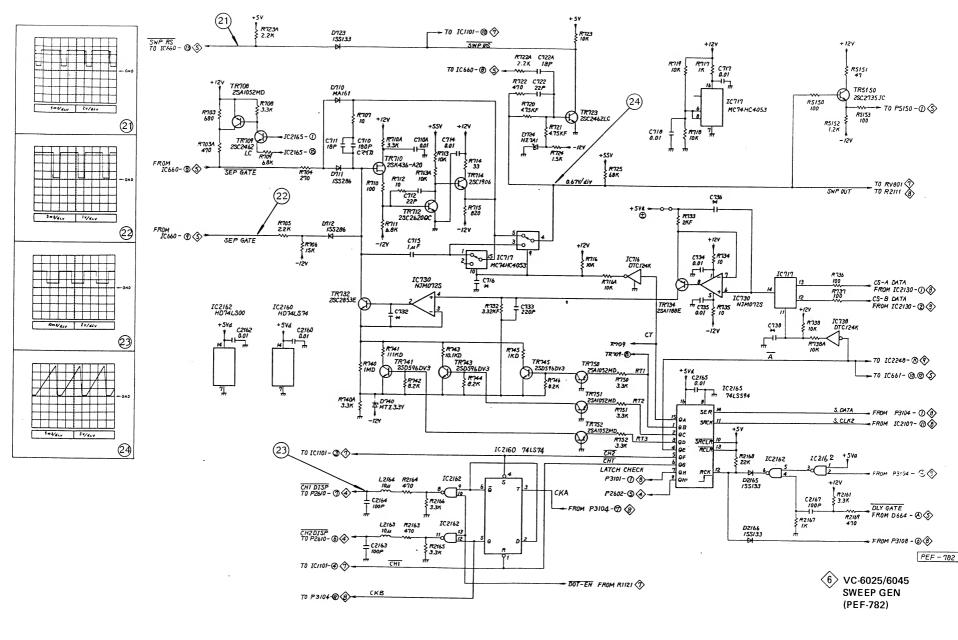


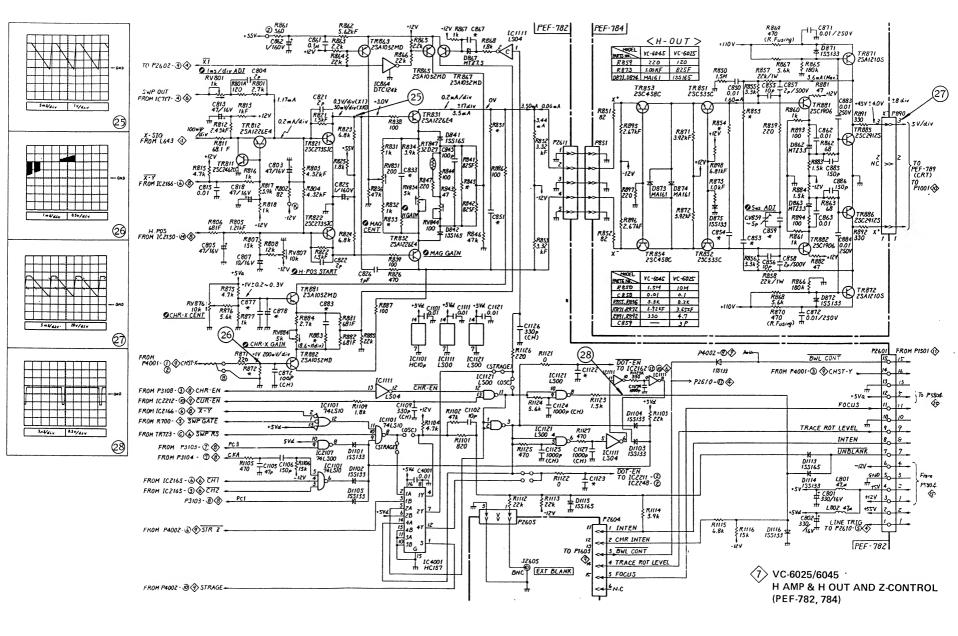


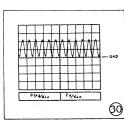


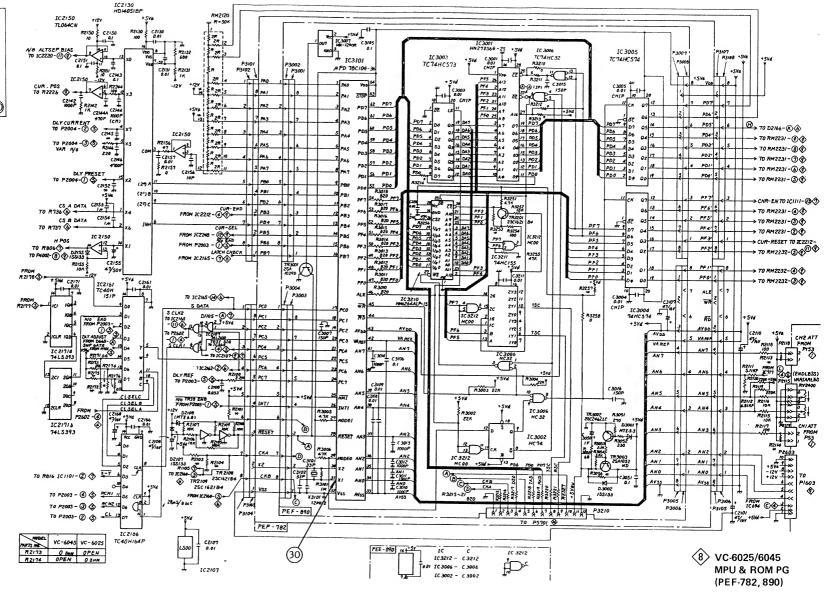


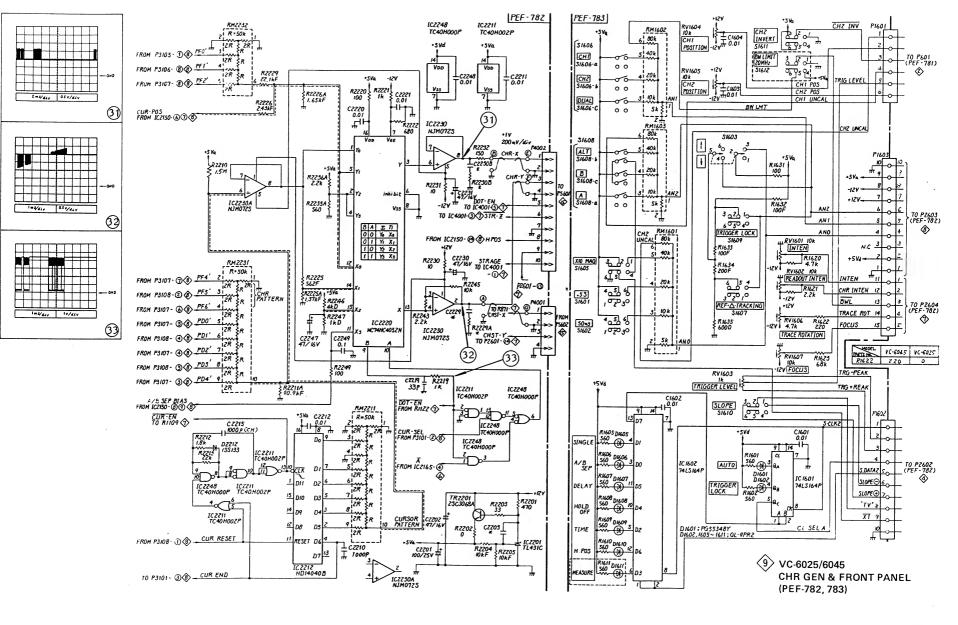


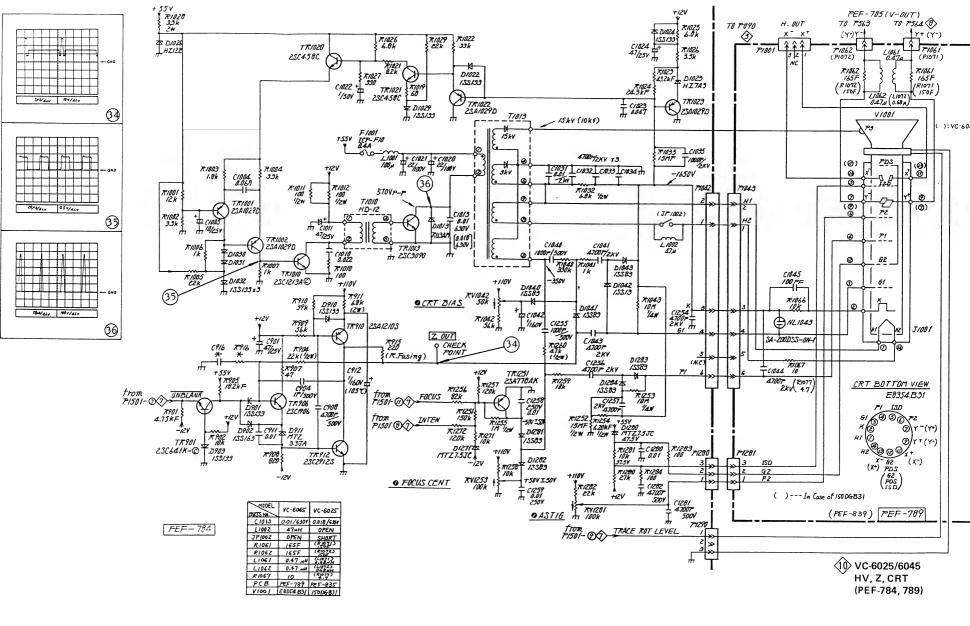


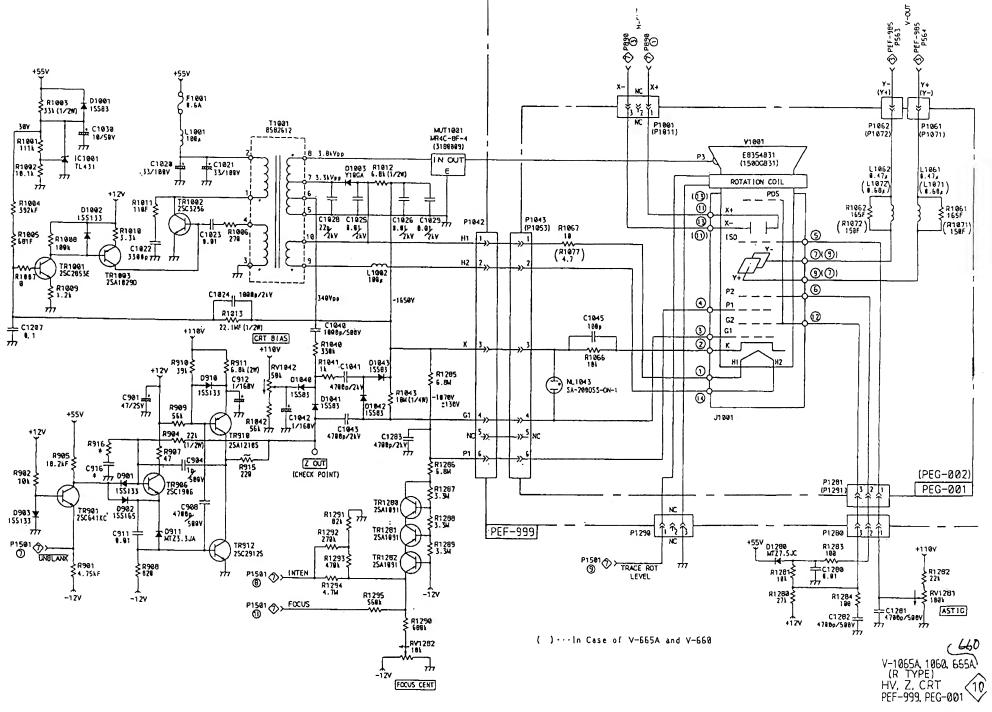


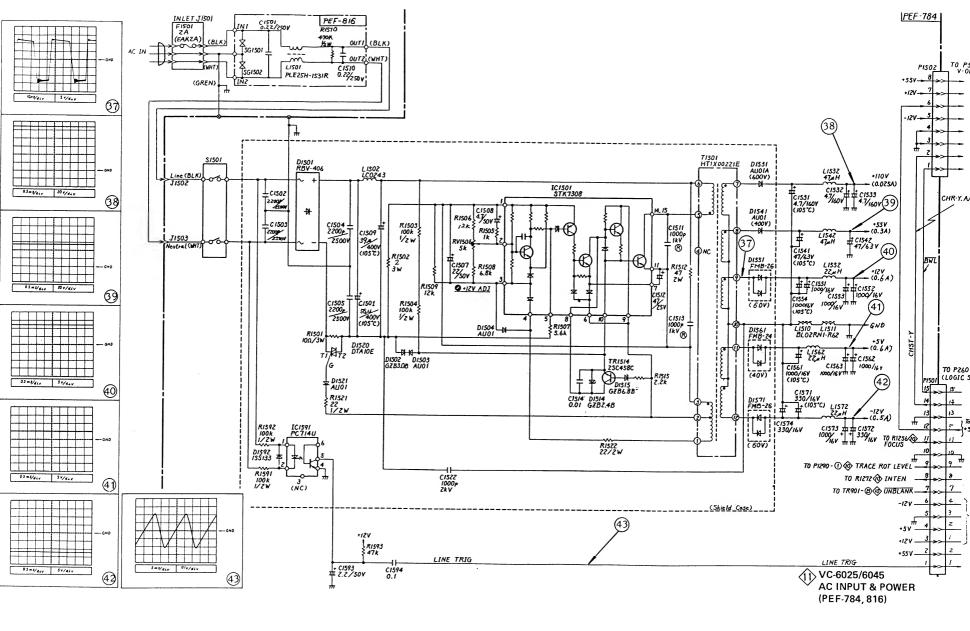




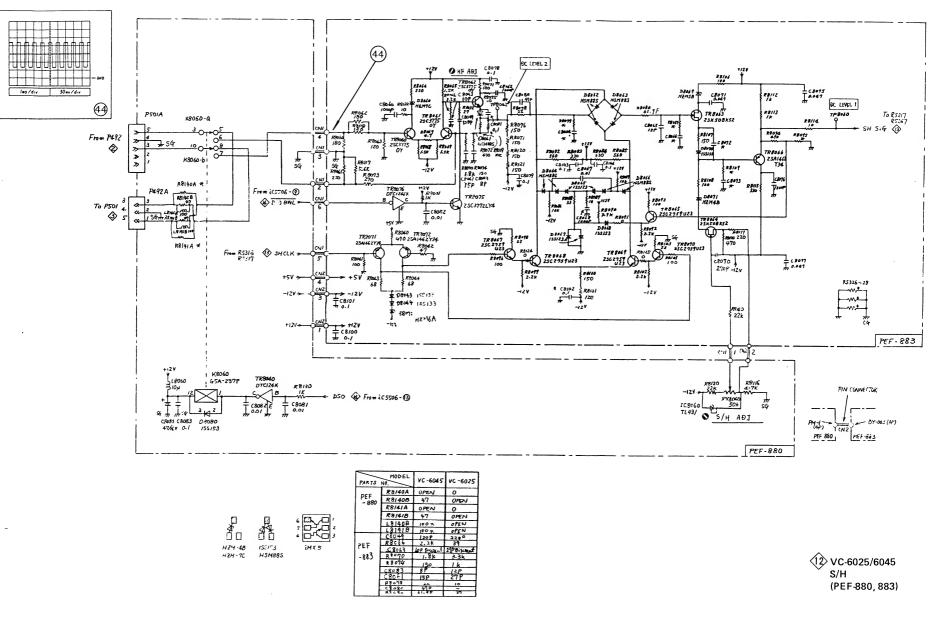


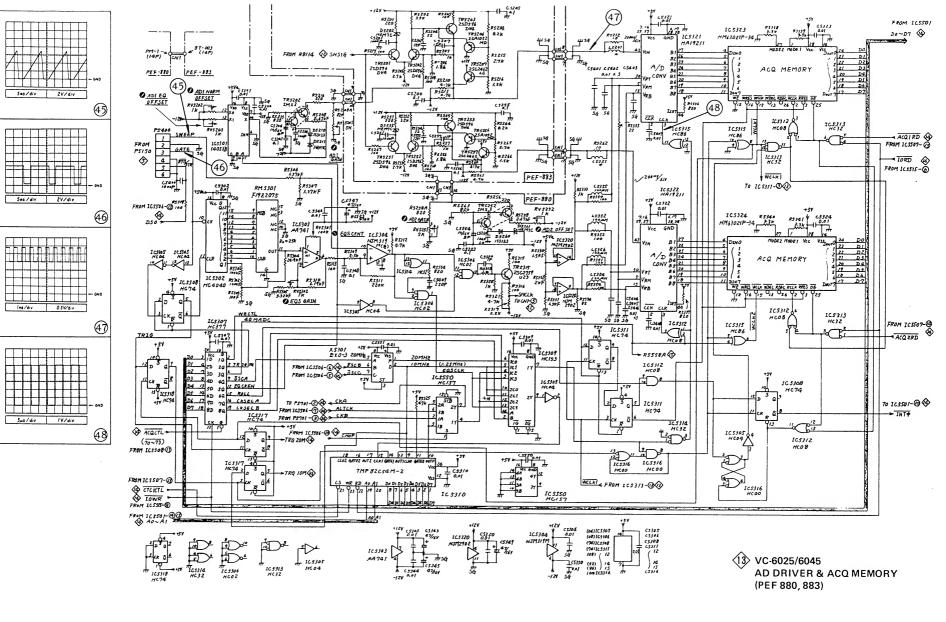




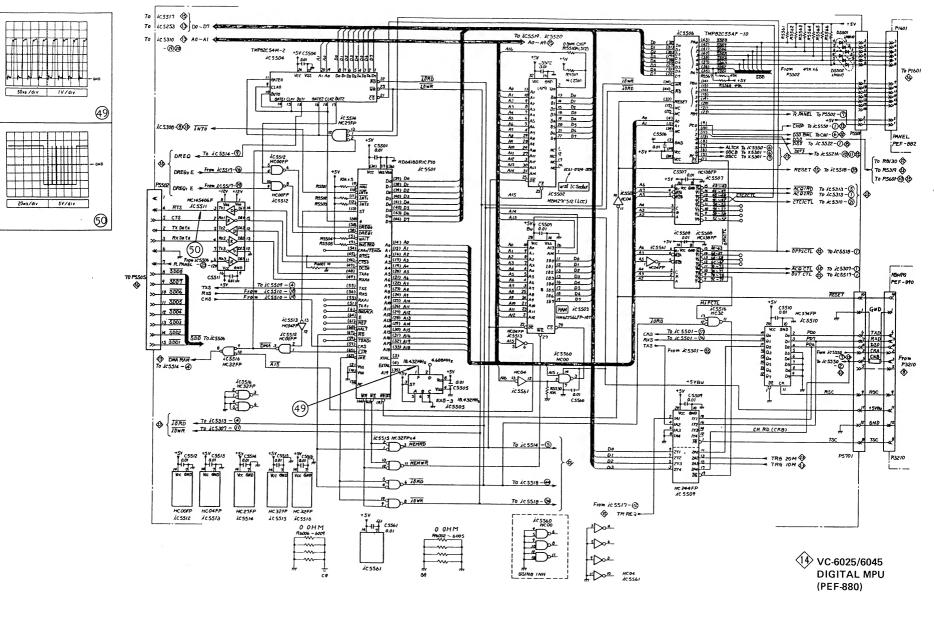


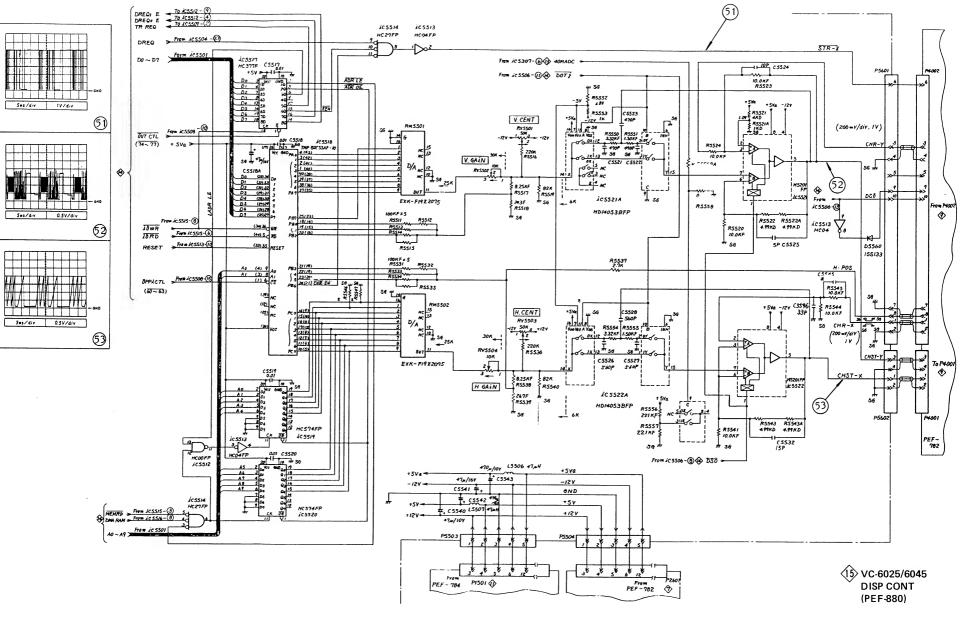
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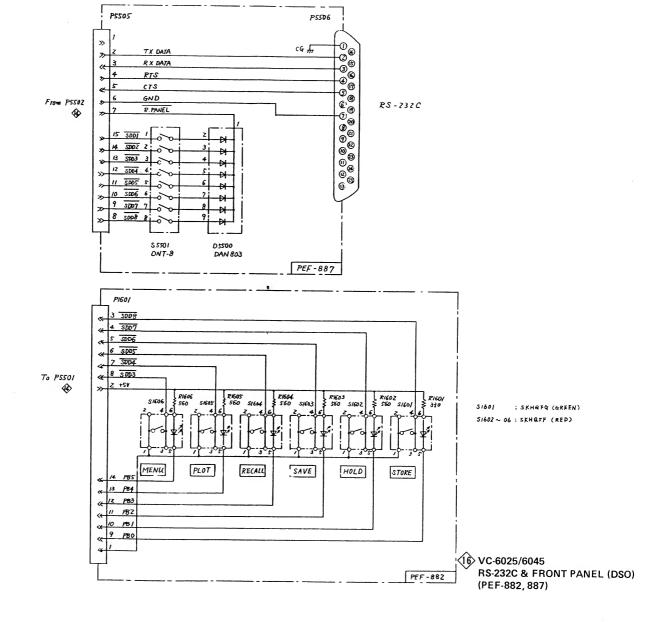




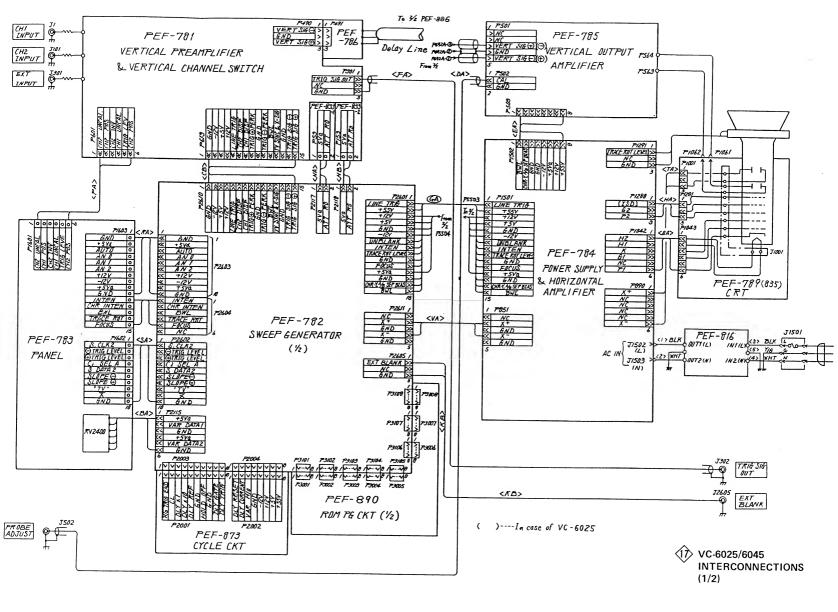
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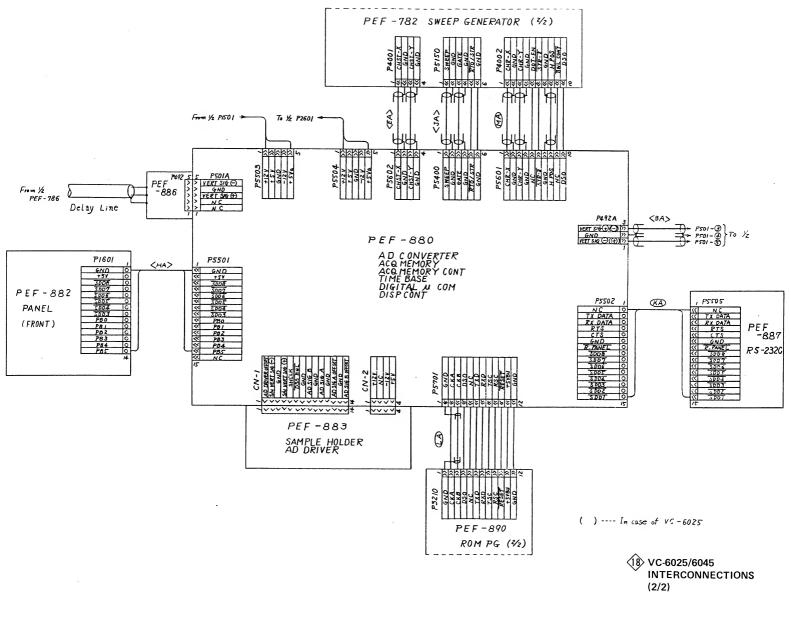






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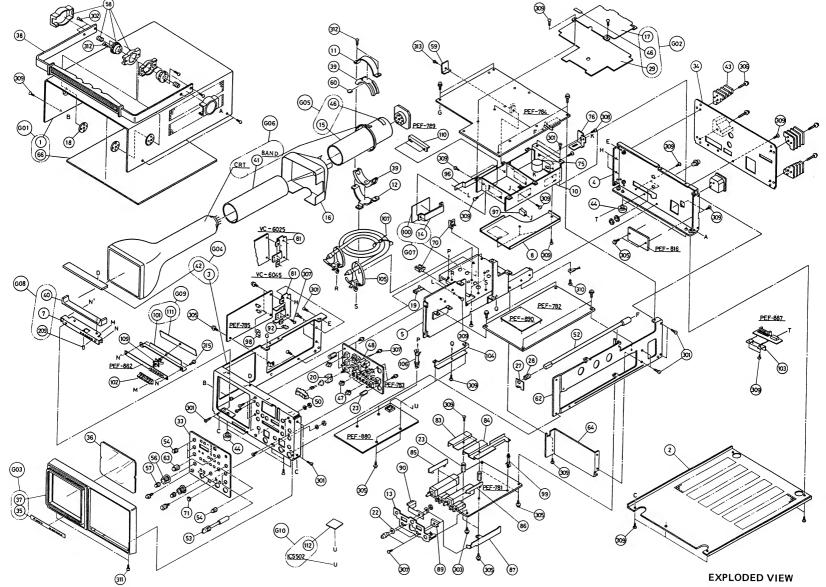


11. MECHANICAL PARTS LIST AND EXPLODED VIEW

A:VC-6025 B: VC-6045

G01 62M0028 TOP Cover Assy 1 G02 62M0029 Shield Case Assy 1 G03 62M0026 Frame Assy 1 G04 62M0026 Frame Assy 1 G04 62M0024 Shield Band Assy 1 G05 62M0027 Shield Band Assy 1 G06 62X0005 CRT Assy 1 G06 62X0006 CRT Assy 1 G06 62X0005 CRT Assy 1 G07 62X0025 HIC Bracket Assy 1 G08 62X0007 Seat Assy 1 1 G09 62M0032 Support Bracket Assy 1 1 G10 62X0007 Seat Assy 1 1 2 3225299 A Bottom Cover 1 1 2 3224311 B Rear Chassis 1 1 7 2127782 A C Chassis 1 1 1 8483085 A HV Cover 1 1 1 8488097 A CRT Band (1) 1 1			A:VC-6025	в:	VC-604	
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302	XCA7410	Screw Flat 4x10	4	4
303	8340167 M	Screw Sems 3x6	2	2
305	XCA0661	Screw Sems 3x8	37	37
306	8340167 C	Screw Sems 4x20	4	4
307	XCA6205	Screw2x5Screw3x8Screw4x8ScrewBlackScrew3x16Screw3x6	8	8
309	XCA6308		25	25
310	XCA6408		1	1
311	XCA1818		2	2
312	XCA6316		6	6
315	XCA6306		2	2



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